Audio Codec ‘97

Revision 2.3 Revision 1.0
April, 2002

NOTICES

Intel Corporation assumes no responsibility for errors or omissions in the guide. Nor does Intel make any commitment to update the information contained herein.

THIS SPECIFICATION IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION OR SAMPLE.

INTEL DISCLAIMS ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO IMPLEMENTATION OF INFORMATION IN THIS SPECIFICATION. INTEL DOES NOT WARRANT OR REPRESENT THAT SUCH IMPLEMENTATION(S) WILL NOT INFRINGE SUCH RIGHTS.

LICENSING

A royalty-free, limited license is available to any interested party who wishes to make use of this Audio Codec '97 specification. Please contact Intel at audio97@intel.com for specific Audio Codec '97 licensing terms.

** Other names and brands may be claimed as the property of others.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. Introduction and Overview

This specification defines the Audio Codec ‘97 (AC ‘97) Architecture and Digital Interface (AC-link) specifically designed for implementing audio and modem I/O functionality in mainstream PC systems. This specification does not explicitly define the companion AC ‘97 Digital Controller component (sometimes referred to or abbreviated as DC ‘97), which typically varies in features and implementation, but is *AC ‘97 compliant* with this specification.

Typical AC ‘97 devices include:

- Audio Codec (often referred to or abbreviated as AC ‘97 or just AC)
- Modem Codec (often referred to or abbreviated as MC ‘97 or just MC)
- Combined Audio/Modem Codec (often referred to or abbreviated as AMC ‘97 or just AMC)

1.1 Audio Codec Feature List

16-bit full-duplex stereo audio Codec (DAC and ADC)

AC ‘97 1.x compliant indicates fixed 48K sampling rate operation (non-extended feature set)

AC ‘97 2.1 compliant indicates extended audio feature set (optional variable rate, multichannel, etc.)

AC ‘97 2.2 compliant indicates extended audio, enhanced riser audio support, and optional S/PDIF

AC’ 97 2.3 compliant indicates extended configuration information and optional jack sensing support

Industry Standard 48-pin QFP package and pinout

Up to four analog line-level stereo inputs; up to two analog line-level mono inputs

High quality pseudo-differential analog CD input

MIC input with 20 dB boost, programmable gain, and AEC reference capability

Dedicated stereo output (LINE_OUT)

Additional stereo output (AUX_OUT) configurable as line level, optional headphone, or optional 4 or 6-ch output

Mono output for speakerphone or internal mono speaker output.

Optional 18- or 20-bit DAC and ADC resolution

Optional output tone and loudness controls

Optional 3D stereo output enhancement

Optional 3rd ADC input channel for dedicated voice input

Optional integrated Sony/Philips Digital Interface (S/PDIF) transmitter for digital output

Comprehensive Power Management capability

Optional Codec Interrupt generation

Extended Codec revision and configuration information

Optional Jack sensing and reporting of connected devices

1.2 Modem Codec Feature List

16-bit full-duplex modem line Codec (DAC and ADC)

AC ‘97 1.x compliant modem indicates proprietary modem functionality (vendor specific feature set)

AC ‘97 2.x compliant modem indicates standardized modem functionality (extended modem feature set)

Vendor specific package

Optional second line modem and handset DACs and ADCs

GPIO and interrupt capability

Comprehensive power management capability

1.3 AC ‘97 Codec Block Diagram

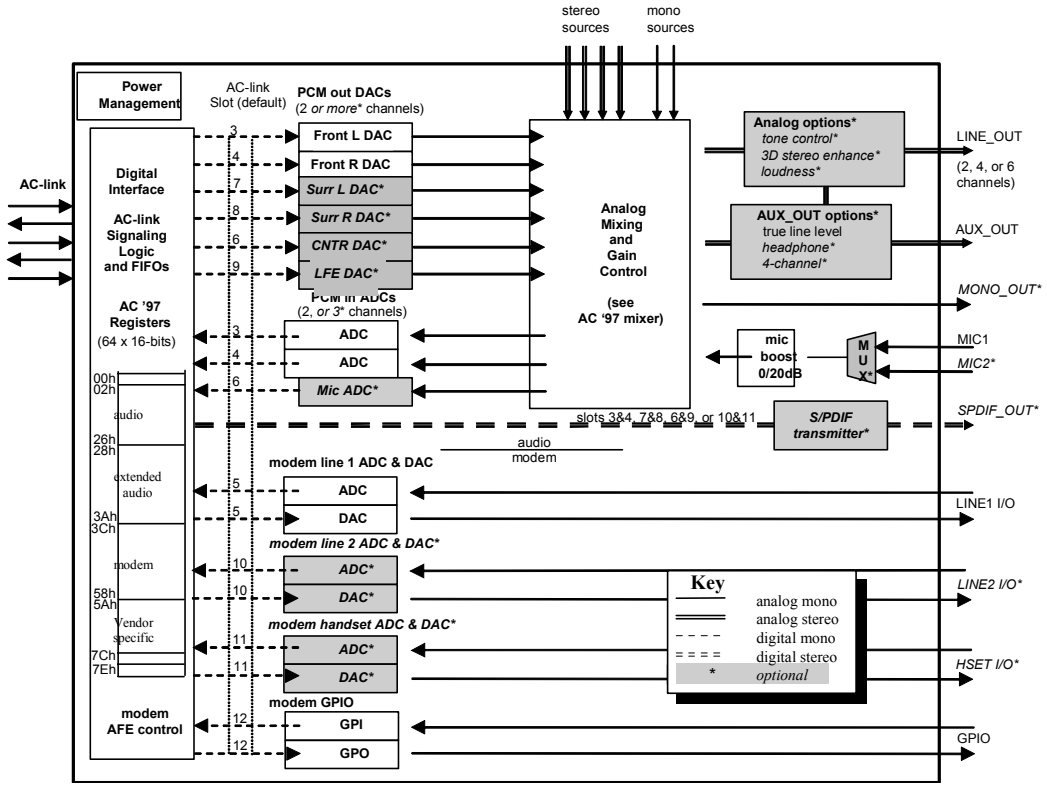


Figure 1. AC ‘97 Codec Block Diagram

Figure 1 shows the functional blocks that make up the AC '97 Codec, which is the analog component of the two-chip AC ‘97 architecture (Controller and Codec — connected by the AC-link digital interface).

The PCM Digital to Analog Converters (DACs) support stereo (optional multichannel) output that contains a mix generated in the AC '97 Controller of all digital audio sources. PCM output is mixed with analog mixer sources, processed with optional 3D stereo enhancement, loudness and tone controls, and sent to LINE_OUT and the independently controlled AUX_OUT, which by default functions as a line level output. AUX_OUT can optionally be configured as headphone or 4-channel output. MONO_OUT was originally designed for analog speakerphone connections, and can be configured to output either microphone only or a mix of sources. For details, refer to Section 5.

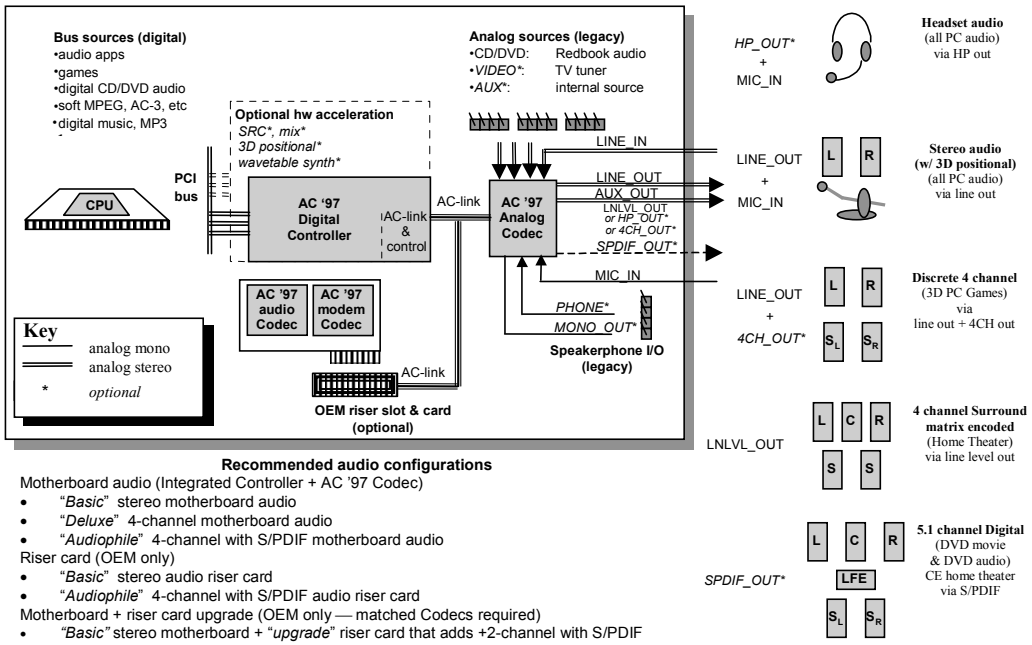
The PCM Analog to Digital Converters (ADCs) support an input capability that can record any mono or stereo

source, or a mix of sources. The optional third PCM ADC is dedicated to voice input, and also extends the range of acoustic echo cancellation (AEC) capabilities. For details, refer to Section 5.

Consumer equipment (CE) compatible digital output is supported via optional SPDIF_OUT. Modem line 1, optional modem line 2, and optional handset ADC/DAC pairs shown in the figure describe integration of modem AFE functionality into the AC '97 architecture. For details, refer to Section 6.

NAMING CONVENTION: Throughout this document signal names have been assigned to be consistent with the point of view of an application running on the PC.

1.4 Integrating AC ‘97 into the System



Recommended audio configurations

Motherboard audio (Integrated Controller + AC '97 Codec)
- “*Basic*” stereo motherboard audio
- “*Deluxe*” 4-channel motherboard audio
- “*Audiophile*” 4-channel with S/PDIF motherboard audio

Riser card (OEM only)
- “*Basic*” stereo audio riser card
- “*Audiophile*” 4-channel with S/PDIF audio riser card

Motherboard + riser card upgrade (OEM only — matched Codecs required)
- *“Basic”* stereo motherboard + “*upgrade*” riser card that adds +2-channel with S/PDIF

Figure 2. AC ‘97 System Diagram

The system diagram in Figure 2 shows the essential features of a typical AC ‘97 system design. The AC ‘97 Codec performs DAC and ADC conversions, mixing, and analog I/O for audio (or modem), and always functions as slave to an AC ‘97 Digital Controller, which is typically either a discrete PCI accelerator or a Controller that comes integrated within core logic chipsets.

The digital link that connects the AC ‘97 Digital Controller to the AC ‘97 Codec, referred to as AC-link, is a bi-directional, 5-wire, serial time domain multiplexed (TDM) format interface. AC-link supports connections between a single Controller and up to 4 CODECs on a circuit board and/or riser card. For details, refer to Section 3.

The system diagram illustrates many of the common PC audio connections, both digital and analog. PC audio today is rapidly moving towards a *Digital Ready* architecture that requires all audio sources must be available in digital form, but a number of legacy analog sources still require the support of an analog mixing stage.

The AC ‘97 architecture supports a variety of audio output options, including:

- **Analog stereo output** (LINE_OUT) transmitted to amplified stereo PC speaker array via stereo mini-jack.

- **Amplified analog stereo headphone output** (HP_OUT) transmitted to headphones or headset via stereo mini-jack.
- **Discrete analog 6-channel output** (LINE_OUT plus 4CH_OUT) transmitted to Front and Surround amplified stereo PC speaker arrays via three stereo mini-jacks.
- **Analog matrix-encoded Surround output** (such as Dolby ProLogic**) transmitted via stereo line level output jack (LNLVL_OUT) or an amplified output (AUX_OUT or HP_OUT) to consumer A/V equipment that drives a home theater multi-speaker array.
- **Digital 5.1 channel output** (such as Dolby Digital** AC-3) transmitted via S/PDIF (SPDIF_OUT) to digital ready consumer A/V equipment which drives a home theater multi-speaker array.

1.5 Driver Support for AC ‘97 Controller/Codec Interoperability

As mentioned previously, this specification does not explicitly define the companion AC ‘97 Digital Controller component. However, any driver written for an AC ‘97 Controller/Codec pairing is responsible for exposing and managing an AC ‘97 Codec’s features. Cross-vendor Controller/Codec interoperability requires that, at a minimum, an AC ‘97 driver identifies and supports the following AC ‘97 feature set:

- 16-bit stereo output — slot 3&4 signaling, sample rate conversion (SRC), and DACs
- 16-bit mono or stereo input — slot 3&4 signaling, SRC, ADCs, and microphone selection, boost/gain
- AC ‘97 mixer — analog input sources, levels and mutes, LINE_OUT and AUX_OUT levels
- Power management

Every AC ‘97 Controller/Codec pairing must include the capability (in either the Controller, Codec, or driver) to perform high quality[1] digital SRC in support of stereo output and input at the following sample rates. For mainstream PC systems, it is recommended that every AC ‘97 Controller/Codec pairing include this SRC capability *in hardware*:

- 8.0, 11.025, 16.0, 22.05, 32.0, 44.1, and 48 kHz

It is also recommended that all AC ‘97 drivers support the following common *optional* AC ‘97 features, when determined to be present in the AC ‘97 Codec:

- Tone control
- SRC for the rates listed above
- Loudness
- 3D stereo enhancement
- AUX_OUT configured as true line level or headphone output

Other optional features may require specific support in the AC ‘97 Controller. In these cases interoperability may be limited to an AC ‘97 Controller/Codec pairing where the CODECs are sourced by the same vendor:

- Multichannel (4- or 6-channel) audio
- 20 bit sample size
- S/PDIF digital output
- Third ADC for dedicated voice input
- Modem ADC, DAC and GPIO
- Multiple audio Codecs
- Docking functionality
- Vendor-specific features

[1] AC ‘97 compliance requires that the digital SRC capability located in the Controller, Codec, or software driver meet or exceed the following:

- ≥ 85 dB FS A dynamic range
- ≥ 17.64 kHz -3 dB frequency response
- ≤ -70 dB FS passband THD+N
- ≤ 0.5 dB passband ripple

2. Package, Pinout, and Signal Descriptions

The 7mm x 7mm 48-pin QFP package originally selected for AC ‘97 audio-only Codecs has become prevalent throughout the industry. Vendors are recommended to follow the 48-pin package pinout assignments as closely as possible. Modem Codec (MC) and Combo Audio/Modem Codec (AMC) packaging and pinouts are entirely vendor specific.

2.1 48-pin QFP package

Figure 3 shows the pinout for the 48-pin QFP package. Figure 4 shows the package mechanicals.

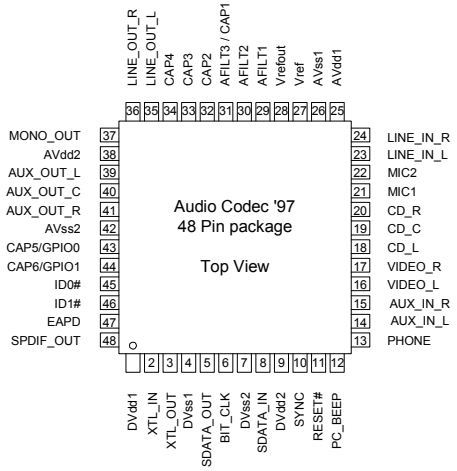
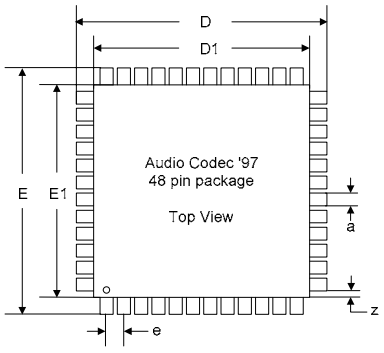


Figure 3. AC ‘97 48-pin package and pinout



Key	Dimension
D	9.00 mm
D1	7.00 mm
E	9.00 mm
E1	7.00 mm
A (lead width)	0.20 mm
e (pitch)	0.50 mm
Z	1.00 mm

Figure 4. AC '97 48-pin package dimensions

2.2 Pinout

Table 1 gives the pinlist for the 48-pin QFP package.

Pin #	Signal Name	Pin#	Signal Name
1	DVdd1	25	AVdd1
2	XTL_IN	26	AVss1
3	XTL_OUT	27	Vref
4	DVss1	28	Vrefout
5	SDATA_OUT	29	AFILT1
6	BIT_CLK	30	AFILT2
7	DVss2	31	AFILT3/CAP1
8	SDATA_IN	32	CAP2
9	DVdd2	33	CAP3
10	SYNC	34	CAP4
11	RESET#	35	LINE_OUT_L
12	Reserved/PC_BEEP	36	LINE_OUT_R
13	PHONE	37	MONO_OUT
14	AUX_IN_L	38	AVdd2
15	AUX_IN_R	39	AUX_OUT_L
16	VIDEO_L	40	AUX_OUT_C
17	VIDEO_R	41	AUX_OUT_R
18	CD_L	42	AVss2
19	CD_C	43	CAP5/GPIO0
20	CD_R	44	CAP6/GPIO1
21	MIC1	45	ID0#
22	MIC2	46	ID1#
23	LINE_IN_L	47	EAPD
24	LINE_IN_R	48	SPDIF_OUT

Table 1. AC '97 48-pin package pinlist

2.3 Signal Descriptions

2.3.1 Power and Ground

It is recommended that the digital portion (logic and AC-link interface) of AC '97 Controllers and Codecs operate at 3.3V (see DC Characteristics in Section 9.1). The analog runs at AVdd = 5V or AVdd = 3.3V.

Pin	Signal Name	Type	Description
1	DVdd1	I	Digital Vdd (3.3V recommended)
4	Dvss1	I	Digital Gnd
7	Dvss2	I	Digital Gnd
9	DVdd2	I	Digital Vdd (3.3V recommended)
25	AVdd1	I	Analog Vdd (5.0V or 3.3V)
26	AVss1	I	Analog Gnd
38	AVdd2	I	Analog Vdd (5.0V or 3.3V)
42	AVss2	I	Analog Gnd

Table 2. Power Signal Descriptions

2.3.2 AC-link and Clocking

These signals connect the AC '97 Codec to its Controller counterpart and external crystal.

Pin	Signal Name	Type	Description
2	XTL_IN	I	24.576 MHz Crystal, 24.576 MHz oscillator or 14.318MHz oscillator input
3	XTL_OUT	O	24.576 MHz Crystal if using crystal as clock source (otherwise Reserved)
5	SDATA_OUT	I	Serial, time division multiplexed, AC '97 Codec input stream from the AC '97 Controller
6	BIT_CLK	O I	Primary Codecs: Master AC-link 12.288 MHz serial data clock output or input Secondary Codecs: Slave Codec 12.288 MHz data clock input
8	SDATA_IN	O	Serial, time division multiplexed, AC '97 Codec output stream to the AC '97 controller
10	SYNC	I	48 kHz fixed rate sample sync
11	RESET#	I	AC '97 Master H/W Reset

Table 3. AC-link and Clocking Signal Descriptions

2.3.3 Digital I/O

These signals are AC '97 Codec digital inputs and outputs.

Pin	Signal Name	Type	Description
43	GPIO0	IO	Optional Vendor specific GPIO
44	GPIO1	IO	Optional Vendor specific GPIO
45	ID0#	I	Codec ID strap pin (or Generic Cap)
46	ID1#	I	Codec ID strap pin (or Generic Cap)
47	EAPD	O	External Amplifier Power Control pin
48	SPDIF_OUT	O	S/PDIF output (or Vendor specific)

Table 4. Digital I/O Signal Descriptions

2.3.3.1 S/PDIF transmitter pin assignment

S/PDIF capable AC ‘97 2.3 Codecs in the standard 48-pin QFP must use pin 48 to implement the S/PDIF output signal. The list of pins that are disabled in the ATE test mode should include the S/PDIF output pin.

In addition, it is suggested that the Codec implement a sensing capability that detects S/PDIF output pin 48 strapped “high” during power up and disables the S/PDIF capability bit in Register 28h. When disabled, the SPSA and SPCV bits in Register 2Ah, and all bits in the S/PDIF Control Register 3Ah should return “0” when read. This optional feature allows system designers to populate or depopulate S/PDIF connector hardware, while maintaining automatic detection in the driver.

2.3.4 Analog I/O

These signals connect the AC ‘97 Codec to analog sources and sinks, including microphones and speakers.

Pin	Signal Name	Type	Description
12	Reserved / PC_BEEP	I	PC Beep if implemented as external input; otherwise, Reserved
13	PHONE	I	Speakerphone Input
14	AUX_IN_L	I	Aux Input Left Channel
15	AUX_IN_R	I	Aux Input Right Channel
16	VIDEO_L	I	Video Audio Input Left Channel
17	VIDEO_R	I	Video Audio Input Right Channel
18	CD_L	I	CD Audio Input Left Channel
19	CD_C	I	CD Audio Common
20	CD_R	I	CD Audio Input Right Channel
21	MIC1	I	Primary Microphone Input
22	MIC2	I	Secondary Microphone Input
23	LINE_IN_L	I	Line Input Left Channel
24	LINE_IN_R	I	Line Input Right Channel
35	LINE_OUT_L	O	Line Output Left Channel
36	LINE_OUT_R	O	Line Output Right Channel
37	MONO_OUT	O	Speakerphone Output or internal mono speaker output
39	AUX_OUT_L	O	Aux Output (LNLVL_OUT, 4CH_OUT or HP_OUT) Left Channel
40	AUX_OUT_C	O	Aux Output (LNLVL_OUT, 4CH_OUT or HP_OUT) Common or AVss
41	AUX_OUT_R	O	Aux Output (LNLVL_OUT, 4CH_OUT or HP_OUT) Right Channel

Table 5. Analog I/O Signal List

2.3.5 Filter/References

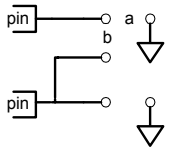
These signals are connected to resistors, capacitors, or specific voltages.

Pin	Signal Name	Type	Description
27	Vref	O	Reference Voltage
28	Vrefout	O	Reference Voltage out 5mA drive (intended for mic bias)
29	AFILT1	O	Anti-Aliasing Filter Cap - ADC channel
30	AFILT2	O	Anti-Aliasing Filter Cap - ADC channel
31	AFILT3	O	Anti-Aliasing Filter Cap - optional Mic ADC channel
31	CAP1	O	Generic Cap
32	CAP2	O	Generic Cap
33	CAP3	O	Generic Cap
34	CAP4	O	Generic Cap
43	CAP5	O	Generic Cap
44	CAP6	O	Generic Cap

Table 6. Filtering and Voltage Reference Signal List

The generic capacitor pins can be used internally to support 3D stereo enhancement, tone control, or other vendor-specific functions. The AC '97 vendor determines the specific use of each capacitor pin. However, to support a vendor-independent AC '97 layout, the following are recommended:

- Internal functions which use generic capacitors between pins should use odd-even (n, n+1) cap pairs, (1-2, 3-4, 5-6, etc.)
- Internal functions that use generic capacitor to ground may use any cap
- Generic capacitor values should be no greater than 1uF (0805 package or smaller is preferred)



To configure capacitor to gnd:

a = capacitor, b = open

To configure capacitor pin to pin:

a = open, b = capacitor

Figure 5. Example of vendor-independent external capacitor layout connection.

3. Controller, Codec, and AC-link

This section describes the physical and high-level functional aspects of the AC ‘97 Controller to Codec interface, referred to as AC-link. For a detailed description of AC-link protocols, slot and bit assignments, refer to Section 4.

3.1 AC-link Physical interface

The AC ‘97 Codec communicates with its companion Digital Controller via the AC-link digital serial interface. AC-link has been defined to support connections between a single Controller and up to four Codecs. All digital audio, modem, and handset data streams, as well as all control (command/status) information are communicated over this serial interconnect, which consists of a clock (BIT_CLK), frame synchronization (SYNC), serial data in (SDATA_IN), serial data out (SDATA_OUT), and a reset (RESET#).

3.2 Controller to Single Codec

The simplest and most common AC ‘97 system configuration is a point-to-point AC-link connection between Controller and Codec, as illustrated in Figure 6.

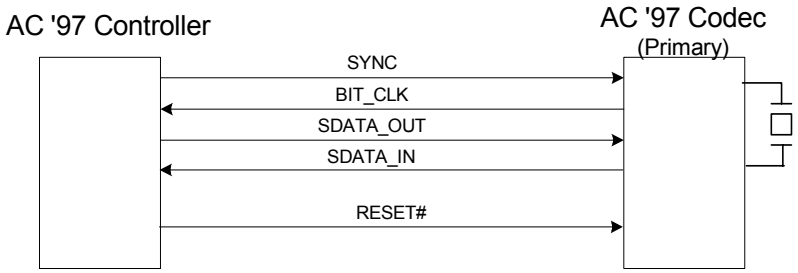


Figure 6. Controller to Codec connections

A primary codec may act as either a source or a consumer of the bit clock, depending on the configuration.

While RESET# is asserted, if a clock is present at the BIT_CLK pin for at least five cycles before RESET# is de-asserted, then the codec is a consumer of BIT_CLK, and must not drive BIT_CLK when RESET# is de-asserted. The clock is being provided by other than the primary codec, for instance by the controller or an independent clock chip. In this case the primary codec must act as a consumer of the BIT_CLK signal as if it were a secondary codec.

This clock source detection must be done each time the RESET# line is asserted. In the case of a warm reset, where the clock is halted but RESET# is not asserted, the codec must remember the clock source, and not begin generating the clock on the assertion of SYNC if the codec had previously determined that it was a consumer of BIT_CLK.

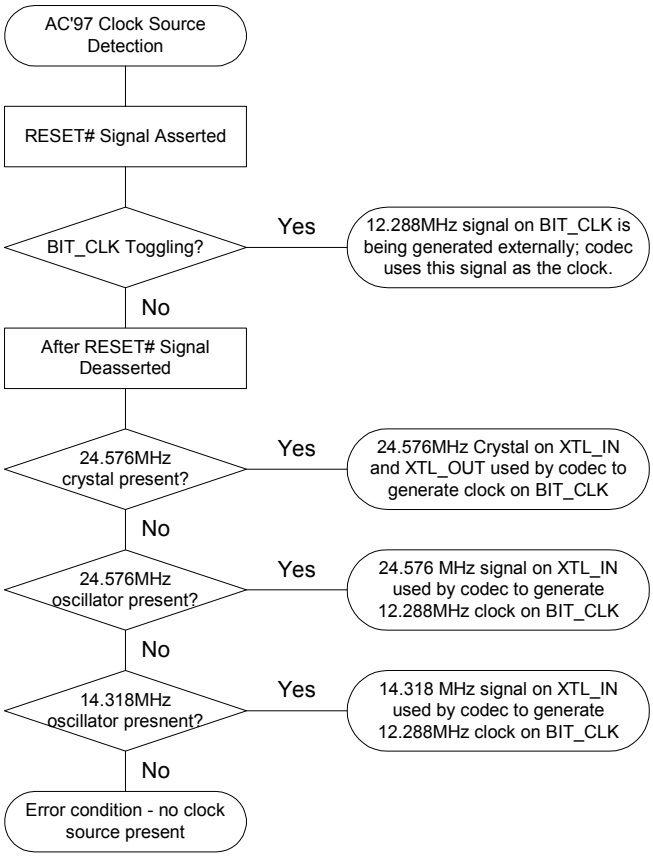


Figure 7. Codec Clock Source Detection[2]

If, when the RESET# signal has been de-asserted, the codec has not detected a signal on BIT_CLK as defined in the previous paragraph then the AC '97 Codec derives its clock internally from an externally attached 24.576 MHz crystal[3] or oscillator, or optionally from an external 14.318MHz oscillator[4], and drives a buffered 12.288MHz clock to its digital companion Controller over AC-link under the signal name "BIT_CLK". Clock jitter at the DACs and ADCs is a fundamental impediment to high quality output, and the internally generated clock will provide AC '97 with a clean clock that is independent of the physical proximity of AC '97's companion Digital Controller (henceforth referred to as "the Controller").

If BIT_CLK begins toggling while the RESET# signal is still asserted, the clock is being provided by other than the primary codec, for instance by the controller or by a discrete clock source. In this case, the primary codec must act as a consumer of the BIT_CLK signal as if it were a secondary codec.

[2] This figure is for reference of end states only, and is not intended to imply an actual detection sequence. The actual flow of the detection is left up to the codec manufacturer.
[3] The use of crystal is recommended, but an external oscillator may also be input to AC '97 XTAL_IN
[4] The mechanism used to determine whether a 14.318MHz or other oscillator is attached to the primary codec is not currently defined, and is left up to each codec manufacturer. This may be specified in the future revisions of this specification.

The beginning of all audio sample packets, or Audio Frames, transferred over AC-link is synchronized to the rising edge of the SYNC signal. SYNC is driven by the Controller. The Controller generates SYNC by dividing BIT_CLK by 256 and applying some conditioning to tailor its duty cycle. This yields a 48 kHz SYNC signal whose period defines an audio frame. Data is transitioned on AC-link on every rising edge of BIT_CLK, and subsequently sampled by the receiving device on the receiving side of AC-link on each immediately following falling edge of BIT_CLK.

3.3 Controller to Multiple Codecs

Several vendor specific methods of supporting multiple Codec configurations on AC-link have been implemented or proposed, including Codecs with selective AC-link pass-through and controllers with duplicate AC-links. This section defines a standard method for implementing configurations that physically separate AC-link functionality into two or more Codecs, but use a common Digital Controller.

Potential implementations include:

- Multi-channel audio implemented using multiple 2- or 4-channel Codecs
- Separate Codecs for independent audio and modem AFE
- Docking stations, where one Codec is in the laptop and another is in the dock

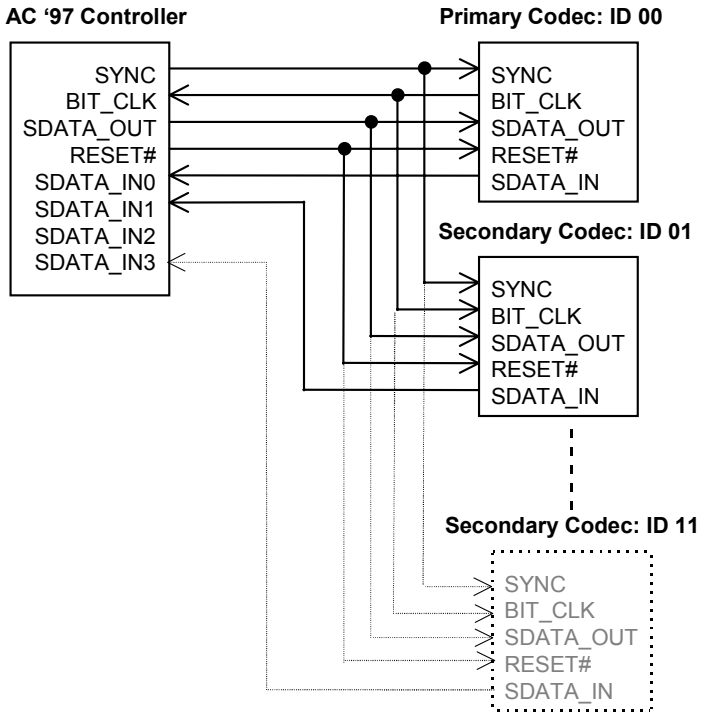


Figure 8. Controller to Multiple Codec connections

This specification defines support for up to four Codecs on the AC-link. By definition there can be one Primary Codec (ID 00) and up to three Secondary Codecs (IDs 01,10, and 11). The Codec ID functions as a chip select. Secondary devices therefore have completely orthogonal register sets; each is individually accessible and they do not share registers.

Multiple Codec AC-link implementations must run off a common BIT_CLK. They can potentially save Controller pins by sharing SYNC, SDATA_OUT, and RESET# from the AC '97 Digital Controller. Each device requires its own SDATA_IN pin back to the Controller. This prevents contention of multiple devices on one serial input line.

Support for multiple Codec operation necessitates a specially designed Controller. An AC '97 Digital Controller that supports multiple Codec configurations implements multiple SDATA_IN inputs, supporting one Primary Codec and up to three Secondary Codecs.

3.3.1 Primary Codec Addressing

Primary AC '97 Codecs respond to register read and write commands directed to Codec ID 00 (see Section 4 for details of the Primary and Secondary Codec addressing protocols). Primary devices must be configurable (by hardwiring, strap pin(s), or other methods) as Codec ID 00, and reflect this in the two-bit Codec ID field(s) of the Extended Audio and/or Extended Modem ID Register(s). See Section 5 for Audio register descriptions and Section 6 for Modem register descriptions.

The Primary Codec may either drive the BIT_CLK signal or consume a signal provided by the digital controller or other clock generator, as defined in section 3.2 and Figure 7. It is recommended that all AC '97 Codecs configurable as Primary be designed to support at least two (optionally up to four) 50 pF signal loads with 10 kΩ input impedance on the BIT_CLK. This ensures that dual (or up to four) Codec implementations will not load down the clock output.

3.3.2 Secondary Codec Addressing

Secondary AC '97 Codecs respond to register read and write commands directed to Codec IDs 01, 10, or 11, see Section 4 for details of the Primary and Secondary Codec addressing protocols. Secondary devices must be configurable (via hardwiring, strap pin(s), or other methods) as Codec IDs 01, 10, or 11 in the two-bit field(s) of the Extended Audio and/or Extended Modem ID Register(s). See Section 5 for Audio register descriptions and Section 6 for Modem register descriptions.

Codecs configured as Secondary must power up with the BIT_CLK pin configured as an input. Using the provided BIT_CLK signal is necessary to ensure that everything on the AC-link is synchronous. BIT_CLK could also potentially be used as the clock source (multiplied by 2 so that the internal rate is 24.576 MHz).

3.3.3 Codec ID Strapping

Audio Codecs in the 48-pin package use pins 45 and 46 (defined as ID0# and ID1#) as strapping (i.e. configuration) pins to configure the Codec ID. The ID0# and ID1# strapping bits adopt inverted polarity and default to 00 = Primary (via a weak internal pullup) when left floating. This eliminates the need for external resistors for Codecs configured as Primary, and maintains backward compatibility with existing layouts that treat pins 45 and 46 as "no connect" or cap to ground. Pulldowns are typically 0-10 kΩ and connected to Digital (not Analog) Ground.

ID1# (pin 46)	ID0# (pin 45)	Configuration
NC	NC	Primary ID 00
NC	pulldown	Secondary ID 01
pulldown	NC	Secondary ID 10
pulldown	pulldown	Secondary ID 11

Table 7. Recommended Codec ID strapping

3.4 Clocking for Multiple Codec Implementations

To keep the system synchronous, all Primary and Secondary Codec clocking must be derived from the same clock source, so they are operating on the same time base. In addition, all AC-link protocol timing must be based on the BIT_CLK signal, to ensure that everything on the AC-link will be synchronous.

The following are potential 24.576 MHz clock options available to a Secondary Codec:

1. Using a common external 24.576 MHz signal source (external oscillator or AC '97 Digital Controller)
2. Using the Primary's crystal out
3. Using the Primary's BIT_CLK output to derive 24.576MHz

3.4.1 Primary AC, MC, or AMC Codec

Primary AC/MC/AMC devices are required to support correctly either of the following clocking options:

1. 24.576 MHz crystal attached to XTAL_IN and XTAL_OUT
2. 24.576 MHz external oscillator provided to XTAL_IN
3. 12.288 MHz oscillator provided to the BIT_CLK input

The Primary device may also optionally support the following clocking option:

4. 14.318 MHz external oscillator provided to XTAL_IN

If a modem Codec is configured as the Primary AC-link Codec, there should not be any Audio Codecs residing on the AC-link (i.e., a modem-only configuration is the only supported configuration for MC '97 as the Primary AC-link Codec).

3.4.2 Secondary AC Codec

Secondary AC devices are required to function correctly using one or more of the following clocking options:

1. 24.576 MHz external oscillator provided to XTAL_IN (synchronous and in phase with Primary 24.576MHz clock)
2. the BIT_CLK input provided by the Primary

3.4.3 Secondary MC Codec

Secondary AC/MC/AMC devices are required to use one or more of the following clocking options to function correctly:

1. The BIT_CLK input provided by the Primary
2. A vendor specified crystal attached to XTAL_IN and XTAL_OUT
3. 24.576 MHz external oscillator provided to XTAL_IN (synchronous with Primary, optionally 3.3Vaux powered)

Regardless of clocking option, Secondary MC Codecs are required to observe AC-link timing synchronous with their BIT_CLK and SYNC inputs. Secondary MC Codecs that utilize clocking option (1) during full power states have a dependency on the accuracy and stability of the BIT_CLK sourced by the Primary AC Codec. Secondary MC Codecs that support wake-up/Caller-ID functionality depend on option (2) or (3) at least during 3.3Vaux powered states. The choice of clocking options (2) vs. (3) can have an impact on sleep state power consumption.

3.4.3.1 Special AC + MC considerations

A multiple Codec audio plus modem configuration typically would want to target the highest quality audio while also supporting D3 cold wake-up modem capabilities. Highest quality audio mandates clean AVdd and DVdd voltage sources for the audio Codec, while modem power management (D3 wake) capabilities dictates being powered by Vaux. Given this there may be cases when it makes sense to supply a free running high-speed clock to both Codecs. In this way all Codecs can be independently power managed without any problems that would be

associated with being dependent on some other Codec's clock being active. The AC '97 Digital Controller could be designed to manage power to the source of the high-speed clock.

3.5 AC-link Power Management

3.5.1 Powering down the AC-link

The AC-link signals can be placed in a low power mode. When AC '97's Powerdown Register (26h) is programmed to the appropriate value, both BIT_CLK and SDATA_IN are brought to and held at a logic low voltage level. After signaling a reset to AC '97, the AC '97 Controller should not attempt to play or capture audio data until it has sampled a Codec Ready indication from AC '97.

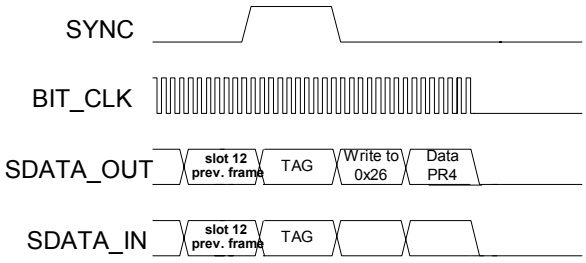


Figure 9. AC-link Powerdown Timing

BIT_CLK and SDATA_IN are transitioned low immediately following decode of the write to the Powerdown Register (26h) with PR4. When the AC '97 Controller driver is at the point where it is ready to program the AC-link into its low power mode, slots 1 and 2 ARE ASSUMED TO BE the only valid stream in the audio output frame[5].

After programming the AC '97 device to this low power, halted mode, the AC '97 Controller is required to drive and keep SYNC and SDATA_OUT low.

Once the AC '97 Codec has been instructed to halt BIT_CLK, a special "wake-up" protocol must be used to bring the AC-link to the active mode since normal audio output and input frames can not be communicated in the absence of BIT_CLK.

3.5.2 Waking up the AC-link

There are two methods for bringing the AC-link out of a low power, halted mode. Regardless of the method, it is the AC '97 Controller that performs the wake-up task.

3.5.2.1 Controller Initiates Wake-up

AC-link protocol provides for a "Cold AC '97 Reset", and a "Warm AC '97 Reset" (see Section 3.6). The current powerdown state would ultimately dictate which form of AC '97 reset is appropriate. Unless a "cold" or "register" reset (a write to the Reset Register) is performed, wherein the AC '97 registers are initialized to their default values, registers are required to keep state during all powerdown modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of four audio frame times following the frame in which the powerdown was triggered. When AC-link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

[5] At this point in time it is assumed that all sources of audio input have also been neutralized.

3.5.2.2 Codec Initiates Wake-up

A Codec (running off Vaux) can trigger a wake event (PME#) by transitioning SDATA_IN from low to high and holding it high until either a warm or cold reset is observed on the AC-link. This functionality is typically implemented in modem Codecs that detect ring, Caller ID, etc. For details, see Section 7.

Note that when the AC-link is either programmed to the low power mode or shut off completely, BIT_CLK may stop if the primary codec is supplying the clock, which shuts down the AC-link clock to the Secondary Codec[6]. In order for a Secondary Codec to react to an external event (phone ringing), it must support an independent clocking scheme for any PME# associated logic that must be kept alive when the AC-link is down. This includes logic to asynchronously drive SDATA_IN to a logic high-level which signals a wake request to the AC '97 Digital Controller. For details, see Section 7.

3.6 Codec Reset

There are three types of AC '97 reset:

- a *cold* reset where all AC '97 logic (registers included) is initialized to its default state
- a *warm* reset where the contents of the AC '97 register set are left unaltered
- a *register* reset which only initializes the AC '97 registers to their default states

3.6.1 Cold AC '97 Reset

A cold reset is achieved by asserting RESET# low for the minimum specified time, then subsequently de-asserting RESET# high. BIT_CLK and SDATA_IN will be activated, or re-activated as the case may be, and all AC '97 control registers will be initialized to their default power on reset values.

RESET# is an asynchronous AC '97 input.

3.6.2 Warm AC '97 Reset

A warm AC '97 reset will re-activate the AC-link without altering the current AC '97 register values. A warm reset is signaled by driving SYNC high for a minimum of 1 µs in the absence of BIT_CLK.

Within normal audio frames SYNC is a synchronous AC '97 input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to AC '97.

AC '97 MUST NOT respond with the activation of BIT_CLK until SYNC has been sampled low again by AC '97. This will preclude the false detection of a new audio frame.

3.6.3 Register AC '97 Reset

All registers in an AC device can be restored to their default values by performing a write (any value) to the Reset Register, 00h. All registers in an MC device can be restored to their default values by performing a write (any value) to the extended modem ID Register, 3Ch. For AMC devices the audio and modem registers should be independently resettable via writes to 00h and 3Ch, respectively.

4. AC-link Digital Interface

4.1 Overview

AC-link is the 5 pin digital serial interface that links AC '97 Codec to Controller. The AC-link protocol is a bi-

[6] Secondary Codec always configures its BIT_CLK pin as an input.

directional, fixed clock rate, serial digital stream. AC-link handles multiple input and output PCM audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme that divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. With a minimum required DAC and ADC resolution of 16-bits, AC '97 could also be implemented with 18 or 20-bit DAC/ADC resolution, given the headroom that the AC-link architecture provides.

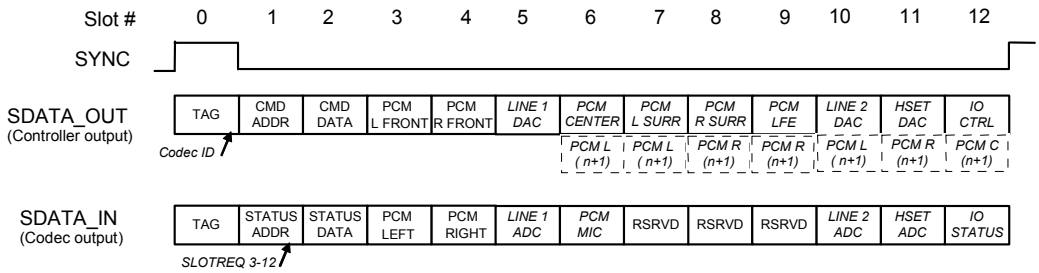


Figure 10. Bi-directional AC-link Frame with Slot assignments

The AC-link output slots (transmitted from the Controller) are defined as follows:

Slot	Name	Description
0	SDATA_OUT TAG	MSBs indicate which slots contain valid data; LSBs convey Codec ID
1	Control CMD ADDR write port	Read/write command bit plus 7-bit Codec register address
2	Control DATA write port	16-bit command register write data
3,4	PCM L&R DAC playback	16, 18, or 20-bit PCM data for Left and Right channels
5	Modem Line 1 DAC	16-bit modem data for modem Line 1 output
6,7,8,9	PCM Center, Surround L&R, LFE	16, 18, or 20-bit PCM data for Center, Surround L&R, LFE channels
10	Modem Line 2 DAC	16-bit modem data for modem Line 2 output
11	Modem handset DAC	16-bit modem data for modem Handset output
12	Modem IO control	GPIO write port for modem Control
10-11	SPDIF Out	Optional AC-link bandwidth for SPDIF output
6-12	Double rate audio	Optional AC-link bandwidth for 88.2 or 96 kHz on L, C, R channels. Actual slots used are controlled by the DRSS bits.

The AC-link input slots (transmitted from the Codec) are defined as follows:

Slot	Name	Description
0	SDATA_IN TAG	MSBs indicate which slots contain valid data
1	STATUS ADDR read port	MSBs echo register address; LSBs indicate which slots request data
2	STATUS DATA read port	16-bit command register read data
3,4	PCM L&R ADC record	16, 18 or 20-bit PCM data from Left and Right inputs
5	Modem Line 1 ADC	16-bit modem data from modem Line1 input
6	Dedicated Microphone ADC	16, 18 or 20-bit PCM data from optional 3rd ADC input
7,8,9	Vendor reserved	Vendor specific (enhanced input for docking, array mic, etc)
10	Modem Line 2 ADC	16-bit modem data from modem Line 2 input
11	Modem handset input ADC	16-bit modem data for modem Handset input
12	Modem IO status	GPIO read port for modem Status

4.2 AC-link Serial Interface Protocol

The AC '97 Controller signals synchronization of all AC-link data transactions. The AC '97 Codec, Controller, or external clock source drives the serial bit clock onto AC-link, which the AC '97 Controller then qualifies with a synchronization signal to construct audio frames. SYNC, fixed at 48 kHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data (Codec for outgoing data and Controller for incoming data) samples each serial bit on the falling edges of BIT_CLK.

The AC-link protocol provides for a special 16-bit time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is tagged invalid, it is the responsibility of the source of the data, (AC '97 Codec for the input stream, AC '97 Controller for the output stream), to fill all bit positions with 0's during that slot's active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase".

Additionally, for power savings, all clock, sync, and data signals can be halted. This requires that an AC '97 Codec be implemented as a static design to allow its register contents to remain intact when entering a power savings mode.

4.2.1 AC-link Variable Sample Rate Operation

The AC-link serial interconnect defines a digital data and control pipe between the Controller and the Codec. The AC-link supports 12 20-bit slots at 48 kHz on SDATA_IN and SDATA_OUT. The time division multiplexed (TDM) "slot-based" architecture supports a per-slot valid tag infrastructure that the source of each slot's data sets or clears to indicate the validity of the slot data within the current audio frame. This tag infrastructure can be used to support transfers between Controller and Codec at any sample rate. If desired, streams can be sent across the AC-link in a negotiated, "tag interleaved" fashion, thereby eliminating the need for up-sampling to a common rate such as 48 kHz.

For audio, AC-link slot interleaved solutions enable the stream of the highest intended quality, either 44.1 or 48 kHz, to be sent along the AC-link with no up-sampling required. Double-rate audio output at 88.2 or 96 kHz is also feasible by combining two output slots per DAC channel. For modem AFE, data streams at a variety of required sample rates can be supported.

4.2.1.1 Variable Sample Rate Signaling Protocol

AC-link's tag infrastructure imposes FIFO requirements on both sides of the AC-link. For example, in passing a 44.1 kHz stream across the AC-link, for every 480 audio output frames that are sent across, 441 of them must contain valid sample data. Does the AC '97 Digital Controller pass all 441 PCM samples followed by 39 invalid slots? Or does the AC '97 Digital Controller evenly interleave valid and non-valid slots? Each possible method brings with it different FIFO requirements. To achieve interoperability between AC '97 Digital Controllers and Codecs designed by different manufacturers, it is necessary to standardize the scheme for at least one side of the AC-link so that the FIFO requirements will be common to all designs. The Codec side of the AC-link is the focus of this standardization.

The new standard approach calls for the addition of "on demand" slot request flags. These flags are passed from the Codec to the AC '97 Digital Controller during every audio input frame. Each time the AC '97 Digital Controller sees one or more of the newly-defined slot request flags set active (low) in a given audio input frame, it knows that it must pass along the next PCM sample for the corresponding slot(s) in the AC-link output frame that immediately follows.

The VRA (Variable Rate Audio) bit in the Extended Audio Status and Control Register must be set to 1 to enable variable sample rate audio operation. Setting the VRA=1 has two functions:

- enables PCM DAC/ADC conversions at variable sample rates by write enabling Sample Rate Registers 2C-34h.
- enables the on demand Codec-to-Controller signaling protocol using SLOTREQ bits that becomes necessary when a DAC's sample rate varies from the 48 kHz AC-link serial frame rate

The table below summarizes the behavior:

AC '97 functionality	VRA=0	VRA=1
SLOTREQ bits	Always 0 (data each frame)	0 or 1 (data on demand)
sample rate registers	forced to 48 kHz	writable

Table 8. VRA Behavior

For variable sample rate output, the Codec examines its sample rate control registers, the state of its FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each AC-link output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits asserted during the current AC-link input frame signal which active output slots require data from the AC '97 Digital Controller in the next audio output frame. An active output slot is defined as any slot supported by the Codec that is not in a power-down state. For fixed 48 kHz operation the SLOTREQ bits are always set active (low) and a sample is transferred in each frame.

For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not. Thus, even in variable sample rate mode, the Codec is always the master: for SDATA_IN (Codec to Controller), the Codec sets the TAG bit; for SDATA_OUT (Controller to Codec), the Codec sets the SLOTREQ bit and then checks for the TAG bit in the next frame.

The VRM (Variable Rate Mic Audio) bit in the Extended Audio Status and Control Register controls the optional MIC ADC input behavior in the same way that VRA=1 controls the PCM ADC.

Note that modem converters (line1, line2, handset) are not affected by the VRA bit, and SLOTREQ bits for active modem DACs are always treated as valid (data on demand).

4.2.1.2 SLOTREQ Behavior and Power Management

SLOTREQ bits for fixed rate, powered down, and all unsupported Slots should be completed with 0s for maximum compatibility with the original AC '97 Component Specification. When a DAC channel is powered down, it disappears completely from the serial frame: output tag and slot are ignored, and the SLOTREQ bit is absent (forced to zero). The SLOTREQ bit should be forced to 1 in the interval between when the power-down bit for its associated channel is turned off and when its channel is ready to accept samples. Controllers can take advantage of this to eliminate the need to poll the AC '97, AMC '97 or MC '97 status registers.

When the Controller wants to power-down a channel, it needs to:

1. Disable source of DAC samples in Controller
2. Set PR bit for DAC channel in Registers 26h, 2Ah, or 3Eh

When the Controller wants to power up the channel, it needs to:

1. Clear PR bit for DAC channel in Registers 26h, 2Ah, or 3Eh
2. Enable source of DAC samples in Controller

4.2.2 Primary and Secondary Codec Register Addressing

The 2-bit Codec ID field in the LSBs of Output Slot 0 is an addition to the original AC-link protocol that enables an AC '97 Digital Controller to independently access Primary and Secondary Codec registers.

For Primary Codec access, the AC '97 Digital Controller:

1. Sets the AC-link Frame valid bit (Slot 0, bit 15)
2. Validates the tag bits for Slot 1 and 2 Command Address and Data (Slot 0, bits 14 and 13)
3. Sets a zero value (00) into the Codec ID field (Slot 0, bits 1 and 0)
4. Transmits the desired Primary Codec Command Address and Command Data in Slots 1 and 2

For Secondary Codec access, the AC '97 Digital Controller:

1. Sets the AC-link Frame valid bit (Slot 0, bit 15)
2. Invalidates the tag bits for Slot 1 and 2 Command Address and Data (Slot 0, bits 14 and 13)
3. Places a non-zero value (01, 10, or 11) into the Codec ID field (Slot 0, bits 1 and 0)
4. Transmits the desired Secondary Codec Command Address and Command Data in Slots 1 and 2

Secondary Codecs disregard the Command Address and Command Data (Slot 0, bits 14 and 13) tag bits when they see a 2-bit Codec ID value (Slot 0, bits 1 and 0) that matches their configuration. In a sense the Secondary Codec ID field functions as an alternative Valid Command Address (for Secondary reads and writes) and Command Data (for Secondary writes) tag indicator.

Secondary Codecs must monitor the Frame Valid bit, and ignore the frame (regardless of the state of the Secondary Codec ID bits) if it is not valid. AC '97 Digital Controllers should set the frame valid bit for a frame with a Secondary register access, even if no other bits in the output tag slot except the Secondary Codec ID bits are set.

4.3 AC-link Output Frame (SDATA_OUT)

The AC-link output frame data streams correspond to the multiplexed bundles of all digital output data targeting AC '97's DAC inputs, and control registers. As mentioned earlier, each AC-link output frame supports up to twelve (12) 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16-bits which are used for AC-link protocol infrastructure.

Figure 11 illustrates the time slot based AC-link protocol.

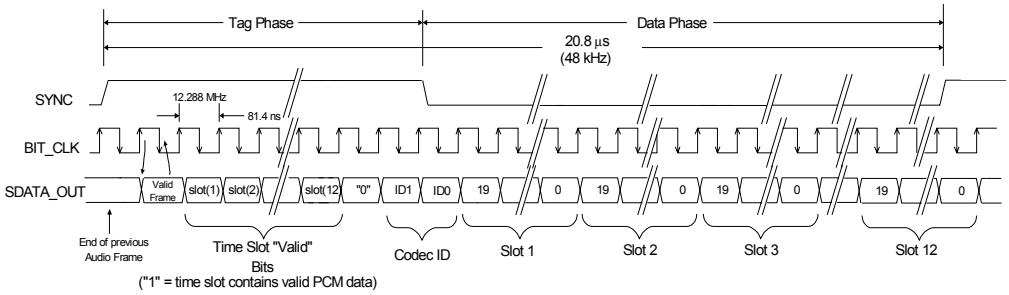


Figure 11. AC-link Output Frame

A new AC-link output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AC '97 Codec samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC '97 Controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC '97 Codec on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

Figure 12. Start of an AC-link Output Frame

SDATA_OUT's composite stream is MSB justified (MSB first) with all non-valid slots' bit positions completed with 0's by the AC '97 Controller. If there are less than 20 valid bits within an assigned and valid time slot, the AC '97 Controller always completes all trailing non-valid bit positions of the 20-bit slot with 0's.

As an example, consider an 8-bit sample stream that is being played out to one of the AC '97 Codec's DACs. The first 8-bit positions are presented to the DAC (MSB justified) followed by the next 12 bit-positions which are completed with 0's by the AC '97 Controller. This ensures that regardless of the resolution of the implemented DAC (16, 18 or 20-bit), no DC biasing will be introduced by the least significant bits.

When mono audio sample streams are output from the AC '97 Controller it is necessary that BOTH left and right sample stream time slots be filled with the same data.

4.3.1 Slot 0: TAG / Codec ID

Bit	Description
15	Frame Valid
14	Slot 1 Primary Codec Valid Command Address bit (Primary Codec only)
13	Slot 2 Primary Codec Valid Command Data bit (Primary Codec only)
12	Slot 3: PCM Left channel Valid Data bit
11	Slot 4: PCM Right channel Valid Data bit
10	Slot 5: Modem Line 1 Valid Data bit
9	Slot 6: PCM Center Valid Data bit
8	Slot 7: PCM Left Surround Valid Data bit
7	Slot 8: PCM Right Surround Valid Data bit
6	Slot 9: PCM LFE Valid Data bit
5	Slot 10: Modem Line 2 or PCM Left (n+1) Valid Data bit
4	Slot 11: Modem Handset or PCM Right (n+1) Valid Data bit
3	Slot 12: Modem GPIO or PCM Center (n+1) Valid Data bit
2	Reserved (Set to 0)
1-0	2-bit Codec ID field (00 reserved for Primary; 01, 10, 11 indicate Secondary)

Table 9. Output Slot 0 Bit Definitions

Within slot 0 the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the "Valid Frame" bit is a 1, this indicates that the current audio frame contains at least one time slot of valid data. The next 12 bit positions sampled by AC '97 indicate which of the corresponding 12 time slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC-link at its fixed 48 kHz audio frame rate.

The two LSBs of Slot 0 transmit the Codec ID used to distinguish Primary and Secondary Codec register access.

4.3.2 Slot 1: Command Address Port

The command port is used to control features, and monitor status (see AC-link input frame Slots 1 and 2) for AC '97 Codec functions including, but not limited to, mixer settings, and power management (refer to the control register section of this specification).

The control interface architecture supports up to sixty-four (64) 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are currently defined, odd register (01h, 03h, etc.) accesses are reserved for future expansion.

Note that shadowing of the control register file on the AC '97 Controller is an option left open to the implementation of the AC '97 Controller. The AC '97 Codec's control register file is nonetheless required to be readable as well as writeable to provide more robust testability.

AC-link output frame slot 1 communicates control register address, and write/read command information to the AC '97 Codec.

Command Address Port bit assignments:

Bit(19)	Read/Write command	(1=read, 0=write)
Bit(18:12)	Control Register Index	(64 16-bit locations, addressed on even byte boundaries)
Bit(11:0)	Reserved	(Stuffed with 0's)

The first bit (MSB) sampled by AC '97 indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be completed with 0's by the AC '97 Controller.

4.3.3 Slot 2: Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle. (as indicated by Slot 1, bit 19)

Bit(19:4)	Control Register Write Data	(Completed with 0's if current operation is a read)
Bit(3:0)	Reserved	(Completed with 0's)

If the current command port operation is a read, then the entire slot time must be completed with 0's by the AC '97 Controller.

4.3.4 Slot 3: PCM Playback Left Channel

AC-link output frame slot 3 is the composite digital audio left playback stream. In a typical 'Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC '97 Controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC '97 Controller must fill all trailing non-valid bit positions within this time slot with 0's.

4.3.5 Slot 4: PCM Playback Right Channel

AC-link output frame slot 4 is the composite digital audio right playback stream. In a typical 'Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC '97 Controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC '97 Controller must fill all trailing non-valid bit positions within this time slot with 0's.

4.3.6 Slot 5: Modem Line 1 Output Channel

AC-link output frame slot 5 contains the MSB justified modem DAC data (if the line Codec is supported). The optional modem DAC resolution is by default 16-bits. During normal runtime operation the AC '97 Controller is then responsible for completing any non-valid trailing bit positions within this time slot with 0's.

4.3.7 Slot 6: PCM Center DAC

Slot 6 carries PCM Center data in 6-channel configurations (either single or multiple Codec implementations).

4.3.8 Slot 7: PCM L Surround DAC (or PCM L n+1)

Slot 7 carries PCM L Surround data in 4- or 6-channel configurations (either single or multiple Codec implementations). This slot may also contain Double Rate Audio data for PCM L n+1 depending on the configuration of the DRSS bits in register 20h.

4.3.9 Slot 8: PCM R Surround DAC (or PCM R n+1)

Slot 8 carries PCM R Surround data in 4- or 6-channel configurations (either single or multiple Codec implementations). This slot may also contain Double Rate Audio data for PCM R n+1 depending on the configuration of the DRSS bits in register 20h.

4.3.10 Slot 9: PCM LFE DAC

Slot 9 carries PCM LFE data in 6-channel configurations (either single or multiple Codec implementations).

4.3.11 Slot 10: Modem Line 2 Output Channel (or PCM L n+1, or S/PDIF output)

AC-link output frame slot 10 contains the MSB justified modem Line 2 DAC data (or extra bandwidth for Double Rate Audio PCM Left, or SPDIF output data).

4.3.12 Slot 11: Modem Handset Output Channel (or PCM R n+1, or S/PDIF output)

AC-link output frame slot 11 contains the MSB justified modem handset DAC data. (or extra bandwidth for Double Rate Audio PCM Right, or SPDIF output data).

4.3.13 Slot 12: Modem GPIO Control Channel (or PCM C n+1)

AC-link output frame slot 12 contains the modem GPIO control outputs (or extra bandwidth for Double Rate Audio PCM Center).

4.3.14 Double Rate Audio in Slots 7, 8 or 10-12

Double Rate Audio is intended to provide AC-link bandwidth (headroom) for future higher end audio implementations where modem is not present. For optional DRA (Double Rate Audio) operation the n+1 sample output slots 7 and 8 or 10-12 must be employed. Setting the Double Rate Audio (DRA=1) bit in the Extended Audio Status and Control Register 2Ah indicates that data from PCM L and PCM R in AC-link output slots 3 and 4 is to be used in conjunction with PCM data on additional slots to provide DAC streams at twice the sample rate designated by the PCM front Sample Rate Control Register 2Ch. The DRSS bits in the General Purpose register specify the slots for the n+1 sample outputs. PCM L (n+1) and PCM R (n+1) data are by default provided in output slots 10 and 11. Multichannel Codecs that support PCM Center additionally combine output slots 6 and 12; the additional Center channel data is not available if the output slots have been set to 7 and 8.

Note that DRA can be used without VRA; in that case the converter rates are forced to 96 kHz if DRA=1.

4.4 AC-link Input Frame (SDATA_IN)

The AC-link input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC '97 Controller. As is the case for audio output frame, each AC-link input frame consists of twelve (12) 20-bit time slots. Slot 0 is a special reserved time slot containing 16-bits which are used for AC-link protocol infrastructure.

The following diagram illustrates the time slot-based AC-link protocol.

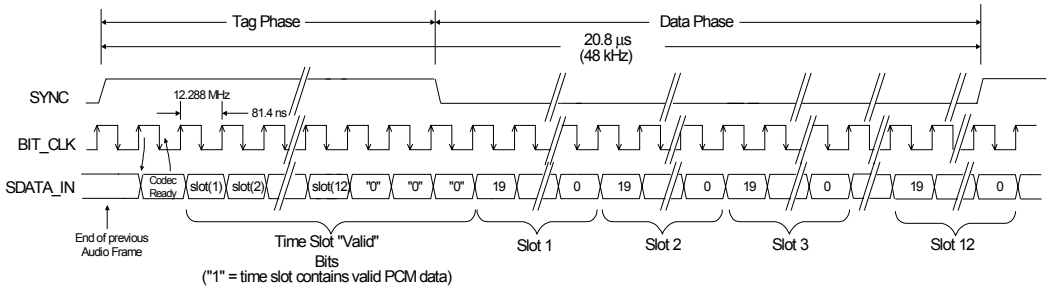


Figure 13. AC-link Input Frame

A new AC-link input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AC '97 Codec samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC '97 Codec transitions SDATA_IN into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC '97 Controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

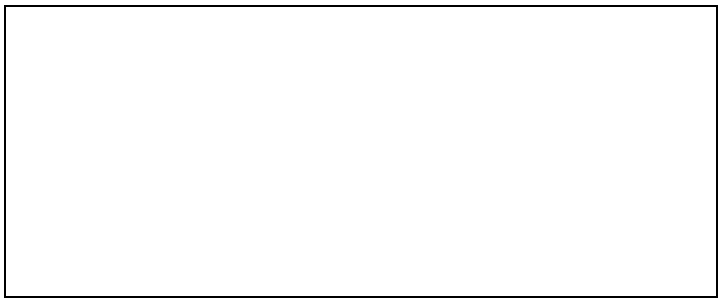


Figure 14. Start of an AC-link Input Frame

SDATA_IN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) filled with 0's by the AC '97 Codec. SDATA_IN data is sampled on the falling edges of BIT_CLK.

4.4.1 Slot 0: TAG

Within slot 0 the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether the AC '97 Codec is in the "Codec Ready" state or not. If the "Codec Ready" bit is a 0, this indicates that the AC '97 Codec is not ready for normal operation. This condition is normal following the deassertion of power on reset - for example, while the AC '97 Codec's voltage references settle. When the AC-link "Codec Ready" indicator bit is a '1,' it indicates that the AC-link and AC '97 Codec control and status registers are in a fully operational state. Codec must assert "Codec Ready" within 400 microseconds after it starts receiving valid SYNC pulses from the controller, to provide indication of connection to the link and Control/Status registers are available for access. The AC`97 Controller and related software must wait until all of the lower four bits of the Control/Status Register, 26h, (Section 5.7.11) are set before attempting any register writes, or attempting to enable any audio stream, to avoid undesirable audio artifacts.

Prior to any attempts at putting an AC '97 Codec into operation the AC '97 Controller should poll the first bit in the AC-link input frame (SDATA_IN slot 0, bit 15) for an indication that the Codec is present and ready by checking for the assertion of the "Codec Ready" bit. Once an AC '97 Codec is sampled "Codec Ready"[7] then the next 12 bit positions sampled by the AC '97 Controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data.

4.4.2 Slot 1: Status Address Port / SLOTREQ signaling bits

Bit	Description
19	RESERVED (Set to 0)
18-12	Control Register Index Echo (Set to 0s if tagged "invalid" by AC '97 Codec)
11-2	On Demand Data Request Flags (next output frame): 0= send data, 1= do NOT send data
11	Slot 3 request: PCM Left channel
10	Slot 4 request: PCM Right channel
9	Slot 5 request: Modem Line 1
8	Slot 6 request: PCM Center
7	Slot 7 request: PCM Left Surround
6	Slot 8 request: PCM Right Surround
5	Slot 9 request: PCM LFE
4	Slot 10 request: Modem Line 2 or PCM Left (n+1)
3	Slot 11 request: Modem Handset or PCM Right (n+1)
2	Slot 12 request: PCM Center (n+1)
1,0	RESERVED (Set to 0)

Table 10. Input Slot 1 Bit Definitions

4.4.2.1 Status Address Port

The status port is used to monitor status for AC '97 Codec functions including, but not limited to, mixer settings and power management. AC-link input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2 (assuming that slots 1 and 2 had been tagged "valid" by the AC '97 Codec

[7] There are several subsections within an AC '97 Codec that can independently go busy/ready. It is the responsibility of the AC '97 controller to probe more deeply into the AC '97 Codec's register file to determine which subsections are actually ready (refer to Section 6.3 for more information).

during slot 0.)

Status Address Port bit assignments:

Bit(19)	RESERVED	(Stuffed with 0)
Bit(18:12)	Control Register Index	(Echo of register index for which data is being returned)
Bit(11:2)	SLOTREQ bits	See next section
Bit(1,0)	RESERVED	(Stuffed with 0's)

The first bit (MSB) generated by AC '97 is always completed with a 0. The following 7 bit positions communicate the associated control register address, the next 10 bits support AC '97's variable sample rate signaling protocol as described in Section 4.2.1.1, and the trailing 2 bit positions are filled with 0's by AC '97.

4.4.2.2 SLOTREQ signaling bits

AC-link input frame Slot #1, the Status Address Port, now delivers Codec control register read address and variable sample rate slot request flags for all output slots. Ten of the formerly reserved least significant bits have been defined as data request flags for output slots 3-12.

The AC-link input frame Slot 1 tag bit is independent of the bit 11-2 slot request field, and ONLY indicates valid Status Address Port data (Control Register Index). The Codec should only set SDATA_IN tag bits for Slot 1 (Address) and Slot 2 (Data) to 1 when returning valid data from a previous register read. They should otherwise be set to 0. SLOTREQ bits have validity independent of the Slot 1 tag bit.

SLOTREQ bits are always 0 in the following cases

- Non-variable rate Codec
- fixed rate mode (VRA=0)
- inactive (powered down) DAC channel (VRA=0 or 1)

SLOTREQ bits are only set to 1 by the Codec in the following case

- Variable rate audio mode (VRA=1) AND active (power ready) DAC AND a non-48 kHz DAC sample rate and Codec does not need a sample

4.4.3 Slot 2: Status Data Port

The status data port delivers 16-bit control register read data.

Bit(19:4)	Control Register Read Data	(Completed with 0's if tagged "invalid" by AC '97)
Bit(3:0)	RESERVED	(Completed with 0's)

If Slot 2 is tagged invalid by AC '97, then the entire slot will be completed with 0's by AC '97.

4.4.4 Slot 3: PCM Record Left Channel

AC-link input frame slot 3 is the left channel output of AC '97's input MUX, post-ADC.

AC '97's ADCs can be implemented to support 16, 18, or 20-bit resolution.

AC '97 ships out its ADC output data (MSB first), and completes any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

4.4.5 Slot 4: PCM Record Right Channel

AC-link input frame slot 4 is the right channel output of AC '97's input MUX, post-ADC.

AC '97's ADCs can be implemented to support 16, 18, or 20-bit resolution.

AC '97 ships out its ADC output data (MSB first), and completes any trailing non-valid bit positions with 0's to fill

out its 20-bit time slot.

4.4.6 Slot 5: Modem Line 1 ADC

AC-link input frame slot 5 contains MSB justified, modem ADC output data (if the line Codec is supported). The optional modem ADC resolution is by default 16-bits. All trailing, non-valid bit positions will be completed with 0’s to fill out its 20-bit time slot. AC ‘97 Controller is then responsible for completing any non-valid trailing bit positions within this time slot with 0’s.

4.4.7 Slot 6: Dedicated Microphone Record Data

AC-link input frame slot 6 is an optional (post-ADC) third PCM system input channel available for dedicated use by a desktop microphone. This input channel would supplement a true stereo output which would then enable a more precise echo cancellation algorithm for speakerphone applications.

AC ‘97’s ADCs can be implemented to support 16, 18, or 20-bit output resolution. Resolution of all PCM input ADC’s, including this optional Mic ADC is reported by the Reset Register. If supported AC ‘97 will ship out ADC data of the implemented resolution (MSB first), and fill any trailing non-valid bit positions with 0’s.

AC ‘97 Controller/AC ‘97 pair interoperability can only be guaranteed for non-optional AC ‘97 audio features. An audio component vendor who develops an AC ‘97 with optional Dedicated Mic channel support should also offer an AC ‘97 Controller to fully support this feature with a matched set solution.

4.4.8 Slots 7-9: Vendor Reserved

AC-link input frame slots 7-9 are reserved for vendor specific use (docking, expanded input capability, array microphone, etc) and are otherwise completed with 0’s by the AC ‘97 Codec.

4.4.9 Slot 10: Modem Line 2 ADC

AC-link input frame slot 10 contains the MSB justified modem Line 2 DAC data.

4.4.10 Slot 11: Modem Handset ADC

AC-link input frame slot 11 contains the MSB justified modem Handset DAC data.

4.4.11 Slot 12: Modem GPIO Status

AC-link input frame slot 12 contains the modem GPIO status inputs.

4.5 AC-link Interoperability Requirements and Recommendations

4.5.1 “Atomic slot” Treatment of Slot 1 Address and Slot 2 Data

Command or Status Address and Data cannot be split across multiple AC-link frames. The following transactions require that valid Slot 1 Address and valid Slot 2 Data be treated as “atomic” (inseparable) with Slot 0 Tag bits for Address and Data set accordingly (that is, both valid):

- AC ‘97 Digital Controller write commands to Primary Codecs
- AC ‘97 Codec status responses

Whenever the AC ‘97 Digital Controller addresses a Primary Codec or an AC ‘97 Codec responds to a read command, Slot 0 Tag bits should always be set to indicate actual Slot 1 and Slot 2 data validity.

Function	Slot 0, bit 15 (Valid Frame)	Slot 0, bit 14 (Valid Slot 1 Address)	Slot 0, bit 13 (Valid Slot 2 Data)	Slot 0, Bits 1-0 (Codec ID)
AC '97 Digital Controller Primary Read Frame N, SDATA_OUT	1	1	0	00
AC '97 Digital Controller Primary Write Frame N, SDATA_OUT	1	1	1	00
AC '97 Codec Status Frame N+1, SDATA_IN	1	1	1	00

Table 11. Primary Codec Addressing: Slot 0 Tag Bits

When the AC '97 Digital Controller addresses a Secondary Codec, the Slot 0 Tag bits for Address and Data must be 0. A non-zero, 2-bit Codec ID in the LSBs of Slot 0 indicates a valid Read or Write Address in Slot 1, and the Slot 1 R/W bit indicates presence or absence of valid Data in Slot 2.

Function	Slot 0, bit 15 (Valid Frame)	Slot 0, bit 14 (Valid Slot 1 Address)	Slot 0, bit 13 (Valid Slot 2 Data)	Slot 0, Bits 1-0 (Codec ID)
AC '97 Digital Controller Secondary Read Frame N, SDATA_OUT	1	0	0	01, 10, or 11
AC '97 Digital Controller Secondary Write Frame N, SDATA_OUT	1	0	0	01, 10, or 11
AC '97 Codec Status Frame N+1, SDATA_IN	1	1	1	00

Table 12. Secondary Codec Addressing: Slot 0 tag bits

4.5.2 Codec Register Status Reads

The following are AC '97 compliance requirements for registers outside of the vendor-defined space (5Ah-7Ah), and AC '97 recommendations for registers within the vendor-defined space. Driver authors should not make any assumptions about vendor-defined space until they have confirmed the manufacturer and revision (Registers 7Ch-7Eh) of the Codec being driven.

- Non-implemented Register Bits: All reserved or non-implemented register bits (marked x in the tables) are required to return 0 when read.
- Non-implemented Addresses: Read access to non-implemented registers are required to echo a 'valid' 7-bit register address in Input Slot 1 and return 'valid' 0000h data in Input Slot 2 on the next AC-link frame.
- Odd Register Addresses: Read (and write) access to odd register addresses are required to be treated the same as non-implemented addresses, instead of aliasing them to the next lower even-numbered register.

4.5.3 Codec Register Status Read Completion Latency

For maximum Controller/Codec interoperability AC '97 compliance requires that Codec register read data be returned in the next AC-link frame following the frame in which the read request occurs.

4.5.4 The Codec-Ready Bit and Audio or Modem DAC/ADC Status Bits

AC '97 compliance requires that Codec-Ready and audio or modem DAC/ADC status bits only change from "ready" to "not ready" in response to a PR state change issued by the Controller to the Powerdown Control/Status Registers 26h, 2Ah, or 3Eh. This ensures that once data is actively flowing on a slot, the Controller or Driver does not have to continuously read the registers to detect any unexpected Codec PR status change.

5. Audio Features

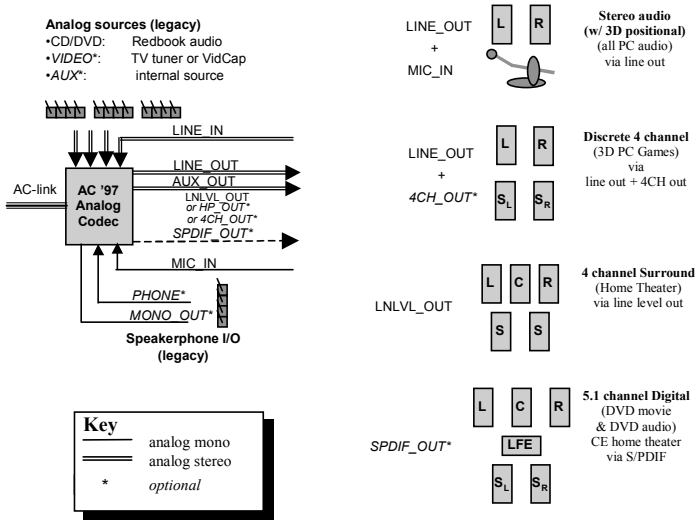


Figure 15. Audio I/O

5.1 Overview

AC '97's PCM Digital to Analog Converters (DACs) support stereo (optional multichannel) output that contains a mix generated in the AC '97 Controller of all digital audio sources. PCM output is mixed with analog mixer sources, processed with optional 3D stereo enhancement, loudness and tone controls, and sent to LINE_OUT and the independently controlled AUX_OUT, which by default functions as a line level output. AUX_OUT can optionally be configured as headphone or 4-channel output.

MONO_OUT was originally designed for analog speakerphone connections, and can be configured as either microphone only or a mix of sources.

The PCM Analog to Digital Converters (ADCs) support an input capability that can record any mono or stereo source, or a mix of sources. The optional third PCM ADC is dedicated to voice input, and also extends the range of acoustic echo cancellation (AEC) capabilities.

Consumer equipment (CE) compatible digital output is supported via optional SPDIF_OUT. Linear PCM or encoded digital formats, such as Dolby Digital** streams are supported via S/PDIF.

The AC '97 architecture supports a variety of audio output options, including:

- *Analog stereo output* (LINE_OUT) transmitted to amplified stereo PC speaker array via stereo mini-jack.

- *Amplified analog stereo headphone output* (HP_OUT) transmitted to headphones or headset via stereo mini-jack.
- *Discrete analog 4-channel output* (LINE_OUT plus 4CH_OUT) transmitted to Front and Surround amplified stereo PC speaker arrays via dual stereo mini-jacks.
- *Analog matrix-encoded Surround output* (such as Dolby ProLogic**) transmitted via stereo line level output jack (LNLVL_OUT) to consumer A/V equipment which drives a home theater multi-speaker array.
- Digital 5.1 channel output (such as Dolby Digital AC-3*) transmitted via S/PDIF (SPDIF_OUT) to digital ready consumer A/V equipment which drives a home theater multi-speaker array.

5.2 LINE_OUT and AUX_OUT

AC ‘97 audio Codecs support two independently controlled stereo outputs:

1. The master output, labeled LINE_OUT, uses pins 35, 36 for L and R (48 pin QFP package) and is controlled by the Master Volume Register 02h. No changes have been made to LINE_OUT definitions.
2. A second output, originally defined as HP_OUT, uses pins 39, 40, and 41 for L, Common, and R (48-pin QFP package) was re-defined as LNLVL_OUT for AC ‘97 2.1, and is controlled by optional volume Register 04h. In addition to the HP and LNLVL definitions, 4-channel Codecs typically utilize pins 39 and 41 for the additional (i.e. L & R Surround) outputs.

5.2.1 AUX_OUT Options

As identified in the previous section, there are three common uses for AC ‘97’s second output. AC ‘97 2.2 addresses all three uses by renaming the second output as AUX_OUT, Register 04h as Aux Out Volume, and the pins as AUX_OUT_L, AUX_OUT_C, and AUX_OUT_R.

Driver developers should be aware that the AC ‘97 AUX_OUT may be implemented in one of three ways:

1. True line level out. Support for a consumer equipment-compatible (10 kΩ) line level output that does not change with master volume settings. Either fixed or fixable via the independent volume controls in Register 04h, the output level provides a 1V RMS (2.8 V peak-to-peak) output level for a 0 dB gain PCM output stream. When implemented this way, AUX_OUT is equivalent to AC ‘97 2.1’s LNLVL_OUT definitions.
2. Headphone out. AUX_OUT can be implemented to support integrated headphone amplifier with 32 Ω drive capability and independent volume control via Register 04h. When implemented this way, AUX_OUT is equivalent to AC ‘97 1.03 original HP_OUT definitions
3. 4-Channel out. In Codecs that support 4-channel operation, AUX_OUT can be implemented to support the additional (i.e. L&R Surround) outputs. When implemented this way, AUX_OUT will be referred to 4CH_OUT. In 4CH_OUT implementations, L and R Surround output is controlled via Surround Volume Register 38h, not Aux Out Volume 04h, and powered down via the PRJ (SDAC) bit in Register 2Ah.

AUX_OUT defaults to be LNLVL_OUT unless HP_OUT or 4CH_OUT support is detected. Unless the specific Codec configuration is indicated via INF file, driver writers should use the following methods for detecting a specialized Codec with HP_OUT or 4CH_OUT capabilities:

- HP_OUT capability can be detected via Reset/ID Register 00h, ID bit 4 and the Aux Out Volume Register 04h default value reads “8000h” (i.e. implemented). ID4 is no longer used to indicate LNLVL support.
- 4CH output capability can be detected via the Extended Audio ID Register 28h, SDAC ID bit 7, and a Surround Volume Register 38h default of “8080h” (i.e. implemented).

HP and LNLVL implementations of AUX_OUT external output are powered down via bit PR6 in Register 26h.

5.3 Audio Sampling Rate Support (Fixed, Variable, and Double)

Fixed 48 kHz audio. All AC ‘97 audio Codecs support 48 kHz fixed sample rate operation, which relies on the Controller or software driver for any sample rate conversion (SRC) capabilities.

Variable rate audio. Variable sample rate audio extends the AC ‘97 architecture to address host-based solutions, similar to those appearing on USB, by minimizing the SRC burden for the primary audio stream. High quality digital SRC and mixing support for both 44.1 and 48 kHz content remain key requirements for supporting multiple

audio sources, regardless of Controller architecture (host-based or hardware-accelerated Controllers).

Double-rate audio. Support is also defined for optional 88.2 or 96 kHz DAC operation. Current PC-based DVD implementations recommend 96 (or 88.2) kHz audio to be down-sampled to 48 (or 44.1) kHz for high quality rendering. However, output slots 10-12 (or optionally slots 7, 8) have been assigned as optional n+1 sample carriers in order to enable double-rate operation on front (L, C, and R) DAC channels with up to 20-bits (120 dB dynamic range) at 88.2 or 96 kHz. Surround and LFE channels remain limited to 48 kHz with up to 20-bits.

5.4 Multichannel Audio

AC '97 assigns AC-link output slots 6-9 for optional multi-channel analog audio. Slots 7 and 8 are dedicated to Surround Left and Surround Right, while Slots 6 and 9 are the Center and LFE channels, respectively. This capability can be used to support multi-channel output from applications such as games, or output multi-channel sound from multi-channel encoded sources such as DVD. This capability can be used in place of, in co-operation with, or entirely independent of, an independent digital stream that may be present on the S/PDIF stream.

5.4.1 Primary Codec Multichannel Audio

A single monolithic AC '97 Codec can support up to 6 channels of analog audio plus fully concurrent S/PDIF using slots 3, 4, 6, 7, 8, 9, 10, and 11 as shown in Figure 16. Volume and mute controls are provided by Registers 02h (L & R), 38h (L & R Surround), and 36h (Center & LFE).

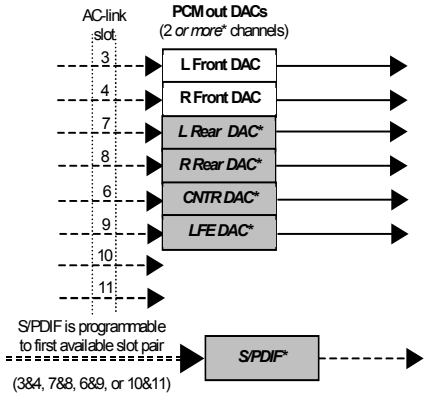


Figure 16. Primary Codec Multichannel implementation

5.4.2 Secondary Codec Multichannel Audio

AC '97 also defines support for multichannel implementations using multiple AC '97 Codecs. Standardized Controller/Codec interoperability (requiring no access to vendor specific registers) depends on two key capabilities:

- mapping of AC-link output slots to DAC functions based on Codec ID
- DAC management, Volume Control and synchronization across multiple Codecs

Intel's recommendation for multiple audio Codec implementations is that the same Codec vendor provides all Codecs. Support for cross-vendor multiple Codec multichannel audio depends on compatibility on details of specific Codec implementation, some of which are not fully addressed by the AC '97 specification.

The following is a partial list of potential cross-vendor multiple Codec multichannel audio compatibility issues

- synchronization
- slot request behavior, start and stop, queue depths, etc.

- SRC mechanisms
- slot mapping configurations
- internal gains and phase inversions

5.4.2.1 Default Slot to DAC Mappings for Secondary Audio Codecs

The AMAP bit, D9 in the Extended Audio ID Register (Register 28h), indicates whether or not the audio Codec supports AC '97 compliant default AC-link slot to audio DAC mappings. AMAP = 1 in D9 indicates that the default (following cold or warm reset) Codec slot to DAC mappings (configured via hardwiring, strap pin(s), or other methods) conform to Table 13.

All Audio Codecs must implement the following power-up default AC-link to DAC mapping behavior:

A Secondary audio Codec by default always assigns its DACs to AC-link slots in a fixed sequence {L, R, LS, RS, C, LFE to 3, 4, 7, 8, 6, 9} with the Codec ID indicating where in the sequence to begin (see table below). Default S/PDIF assignment always begins with the first slots not assigned to DACs.

Optional baseline (see Section 5.8.1) or vendor specific slot to DAC re-mapping capability is also recommended.

Default AC-link to DAC mapping by Codec ID					
Function	Codec ID	3&4	7&8	6&9	10&11
2-ch Primary	00	L&R	–	–	–
2-ch Secondary*	01	–	Surr	–	–
+2-ch Secondary	10	–	Surr	–	–
+2-ch Secondary	11	–	–	C/LFE	–
2-ch Primary with S/PDIF	00	L&R	S/PDIF	–	–
+2-ch Secondary with S/PDIF*	01	–	Surr	S/PDIF	–
+2-ch Secondary with S/PDIF	10	–	Surr	S/PDIF	–
+2-ch Secondary with S/PDIF	11	–	–	C/LFE	S/PDIF
4-ch Primary	00	L&R	Surr	–	–
+4-ch Secondary*	01	–	Surr	C/LFE	–
+4-ch Secondary	10	–	Surr	C/LFE	–
+4-ch Secondary	11	–	-	C/LFE	–
4-ch Primary with S/PDIF	00	L&R	Surr	S/PDIF	–
+4-ch Secondary with S/PDIF*	01	–	Surr	C/LFE	S/PDIF
+4-ch Secondary with S/PDIF	10	–	Surr	C/LFE	S/PDIF
+4-ch Secondary with S/PDIF	11	–	-	C/LFE	S/PDIF
Codec ID is available to the Controller via Register 28h, bits D15 & D14.					
*These new defaults for a Secondary Codec configured as ID 01 replace AC '97 2.1 AMAP recommendations for dock Codec functionality. Since docking is by nature proprietary, the vendor specific support should be used to reconfigure Codec 01 as necessary. All other mappings are compatible with AC '97 2.1 AMAP.					

Table 13. Default Slot to DAC Mappings Based on Codec ID

5.4.2.2 DAC Management across Multiple Audio Codecs

The use of multiple AC '97 Codecs to achieve multi-channel audio requires that the driver writer knows where to access DAC Ready status and Powerdown control for all channels. In monolithic multi-channel Codecs, for Front L&R DACs bit D1 in Register 26h indicates Ready and bit D9 controls Powerdown. For Center, Surround L&R, and LFE channels, bits D6, D7, and D8 in Register 2Ah indicates DAC Ready respectively. Bits D11, D12, and

D13 control Powerdown for the Center, Surround, and LFE DACs respectively.

When a 2-channel Secondary Codec is mapped as Surround L&R, Ready and Powerdown for Surround L&R are not implemented in Register 2Ah, and Register 26h must be used instead.

Similar reasoning can be applied to 6-channel cases: driver writers should check the Secondary Audio Codec Register 28h for SDAC, CDAC, and LDAC ID bits to identify the presence of more than 2 DACs and manage the resources accordingly (i.e. use the corresponding Ready status and Powerdown control bits).

In the case where the codec support the Slot Mapping Registers (Slot Mapping Descriptor, Section 5.9.3), the configuration and mapping of DACs and ADCs to slots across multiple codecs can be optimized by the software to provide the optimum use of available DMA engines, slots, DACs, and external jacks and connections across one or multiple codecs.

5.4.2.3 Volume Control across Multiple Audio Codecs

The use of multiple AC '97 Codecs to achieve multi-channel audio requires that the driver writer knows where to access Volume controls for all four channels. In monolithic multi-channel Codecs, Registers 36h and 38h controls Center/LFE and Surround L&R Volume levels respectively.

When a 2-channel Secondary Codec is mapped as Center/LFE or Surround L&R, neither Register 36 nor 38h are implemented, and in this configuration the Master Volume register 02h must be used instead.

Similar reasoning can be applied to 6-channel cases: driver writers should check the Secondary Audio Codec Register 28h for SDAC, CDAC, and LDAC ID bits to identify the presence of more than 2 DACs and manage the resources accordingly (i.e. use the corresponding Volume Control Register).

5.4.2.4 Playback Synchronization across Multiple Audio Codecs

To establish channel synchronization across multiple audio Codecs at the beginning of playback, AC '97 2.2 recommends that, upon playback start up:

1. Driver clears then sets Powerdown bits (D9 in Register 26h and D11, D12, D13 in Register 2Ah) for all active DAC channels.
2. Driver tags all outgoing slots "invalid" until data has been requested from all active output channels, across all Codecs, then provides the first "valid" data to all active output slots during the same AC-link frame[8].
3. Codecs should be designed to synchronize (i.e. wait for) first "valid" output DAC data, even if it occurs multiple AC-link frames subsequent to the initial data request (SLOTREQ signal).

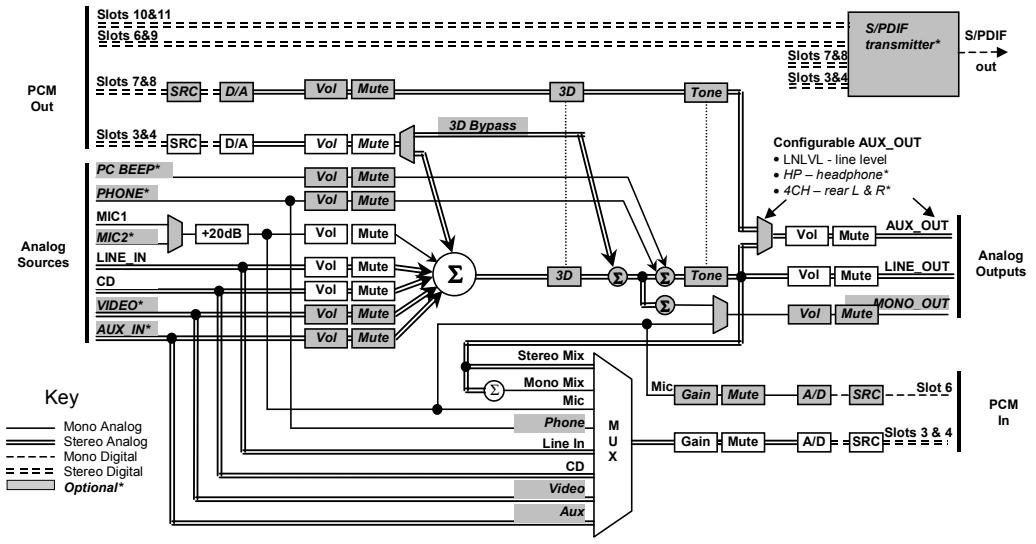
Codecs that do not support synchronization in this manner are limiting themselves to vendor specific driver support (access to vendor specific registers and/or methods) for multichannel upgrades.

5.5 AC '97 Analog Mixer

The AC '97 analog mixer is designed to manage playback and record of all digital and analog audio sources likely to be present in a mainstream PC. These include:

- System audio: digital PCM input and output for business, games, and multimedia
- CD/DVD: analog CD/DVD-ROM Redbook audio with internal connections to Codec mixer
- Mic: choice of desktop or headset microphone, with programmable boost and gain
- Speakerphone: use of system microphone & speakers for telephony, DSVD, and video conferencing
- Line in: external analog line level source from consumer audio, video camera, etc
- Video: TV tuner or video capture card with internal connections to Codec mixer
- AUX: internal analog line level source

[8] Driver writers may also choose to initially transmit several samples of "0000h" (tagged as "valid" data) across all active output slots as an extra multichannel playback start up synchronization measure.



Source	Function	Connection
PCM Out	Digital audio from the AC '97 controller	AC-link
PC_BEEP	PC beep pass thru	From PC beeper output
PHONE	Speakerphone in	From telephony subsystem
MIC1	Desktop microphone	From desktop microphone jack
MIC2	Headset microphone	From headset microphone jack
LINE_IN	External audio source	From line in jack
CD	Audio from CD-ROM drive	Cable from CD-ROM
VIDEO	Audio from TV tuner or video camera	Cable from TV or Video Capture card
AUX_IN	Internal audio source	Internal connector

Destination	Function	Connection
LINE_OUT	Analog mix and front channels	To stereo mini speaker jack
LNLVL_OUT	Fixed line level output	To stereo mini or RCA pair
4CH_OUT	Rear channels	To stereo mini rear speaker jack
HP_OUT	Analog mix and front channels	To stereo mini headphone jack
MONO	Mic or mix for speakerphone out	To telephony subsystem
PCM In	Digital audio input to AC '97 controller	AC-link

Output Mix Supports:
- Stereo mix of all analog sources for line out
- AUX_OUT output configurable as line level, *optional headphone, or optional 4-channel*
- *Optional microphone or mix for mono out*
- *Optional 3D and tone controls*
- *PCM out can be mixed pre or post 3D*

Input Mux Supports:
- Select from 1, 2, or *optionally 3 channels*
- Any mono or stereo source
- Mono or stereo mix of line out
- 2-channel input with output reference (microphone + mono mix)
- *Optional 3rd channel dedicated to microphone*
- *Optional 3-channel input with output reference (microphone + stereo mix)*

Figure 17. AC '97 Mixer Functional Diagram

5.5.1 Analog Mixer Output

The AC '97 mixer generates two distinct outputs:

- a stereo mix of all sources for output to the speakers, headset, and line out (LINE_OUT and HP_OUT)
- a mono "microphone only" or mix of all sources (minus PHONE and PC_BEEP) for speakerphone out (MONO_OUT)

If analog 3D stereo enhancement is supported in AC '97 it is desirable that the PCM out source be mixable pre- or post-analog 3D processing. This allows digital 3D audio (rendered with volume, pan, reverb, Doppler, HRTF, etc.) on PCM out to bypass the analog 3D processing regardless of whether analog 3D is enabled or disabled. This prevents "smearing" of digital 3D audio, and also enables digital 3D audio sources to be mixed with 3D stereo enhanced analog sources (CD, AUX_IN, etc).

The default PCM out path is through volume, mute, and analog 3D stereo enhancement. However, if the AC '97 Controller implements digital 3D audio, and detects analog 3D stereo enhancement support in the AC '97 analog, it can enable the 3D bypass path. This capability to switch to post 3D can also be exposed via API's to support SW which emulates or accelerates digital 3D rendering.

In either PCM out scenario, it is advantageous for the AC '97 Controller to use the post D/A analog volume control

to support full resolution D/A conversions followed by analog attenuation as a means of achieving high SNR.

5.5.2 Analog Mixer Input

The mixer input is a MUX design which offers the capability to record any of the audio sources or the outgoing mix of all sources. This design is more efficient to implement than an independent input mix, allows the user to apply 3D and tone controls to recordings, and offers simple monitoring when a mix is recorded: "what you hear is what you get" (WYHIWYG). Mono and stereo mix also provide echo cancellation reference signals.

AC '97 supports the full range of input options[9]:

- any mono or stereo source
- mono or stereo mix of all sources
- 2-channel input with mono output reference (microphone + mono mix for mono echo cancellation)
- optional 3-channel input with stereo output reference (microphone + stereo mix for stereo echo cancellation)

5.5.3 Analog Mixer Feature Detection

5.5.3.1 Minimum Analog Mixer Feature Set

The following describes the minimum required AC '97 analog mixer feature set, which all AC '97 compliant Codecs support. Drivers are required to support these analog mixer features, which need no audio driver detection:

- Stereo PCM 16-bit DAC playback with volume and mute
- Stereo LINE IN with volume and mute
- Stereo CD with volume and mute
- Mono MIC with 20 dB boost, volume (programmable gain) and mute
- Stereo LINE_OUT with (master) volume and mute
- Stereo AUX_OUT with optional volume and mute
- Stereo PCM 16-bit ADC record with gain and mute

5.5.3.2 Analog Mixer Cost-Reduction

As audio features migrate to digital, some of the original baseline AC '97 analog mixer features will not be needed in future products. In general, if a feature/function is not implemented the following detection protocol can be used: Write all 1's to the appropriate AC '97 register or bit field; if the register or bit field read-back value reads 0, the function is not implemented.

New drivers are recommended to specifically test for presence or absence of support for these, now optional, analog mixer features:

- MONO_OUT (Register 06h, default 8000h)
- PC_BEEP (Register 0Ah, default 0000h or 8000h)
- PHONE (Register 0Ch, default 8008h)
- VIDEO (Register 14h, default 8808h)
- AUX_IN (Register 16h, default 8808h)
- MIC2 (Register 20h, bit 8, default 0)

5.5.3.3 Original Analog Mixer Options

The following AC '97 analog mixer features have always been optional to implement, and have feature ID bits in the Reset/ID (00h) Register. Drivers are recommended to specifically test for presence or absence of support for these optional analog mixer features:

- Dedicated Mic ADC input channel (Register 00h, bit 0)
- Reserved (Register 00h, bit 1)
- Bass and treble control (Register 00h, bit 2)
- Simulated mono to stereo (Register 00h, bit 3)

[9] The audio driver should maintain a persistent record input level for each MUX input option.

- Headphone (Register 00h, bit 4)
- Loudness or bass boost (Register 00h, bit 5)
- 18-bit DAC resolution (Register 00h, bit 6)
- 20-bit DAC resolution (Register 00h, bit 7)
- 18-bit ADC resolution (Register 00h, bit 8)
- 20-bit ADC resolution (Register 00h, bit 9)

5.6 Slot Assignments for Audio

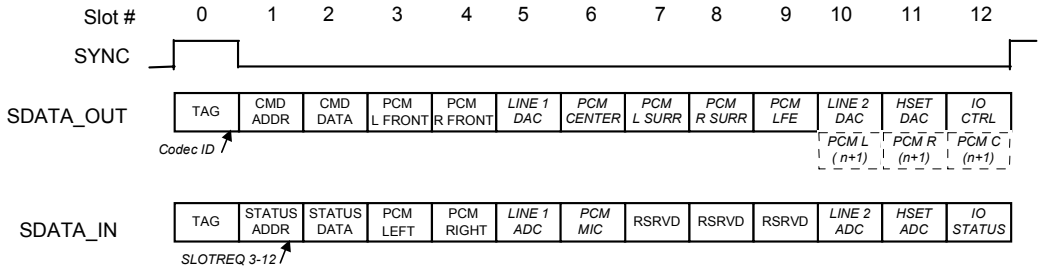


Figure 18. AC-link Slot Definitions

The AC-link output slots dedicated to audio are defined as follows:

Slot	Name	Description
3	PCM L DAC playback	16, 18, or 20-bit PCM data for left channel
4	PCM R DAC playback	16, 18, or 20-bit PCM data for right channel
6	PCM Center	16, 18, or 20-bit PCM data for Center channel
7	PCM L Surround	16, 18, or 20-bit PCM data for L Surround channel
8	PCM R Surround	16, 18, or 20-bit PCM data for R Surround channel
9	PCM LFE	16, 18, or 20-bit PCM data for LFE channel
10	Double rate audio	Optional AC-link bandwidth for 88.2 or 96 kHz on PCM L channel
11	Double rate audio	Optional AC-link bandwidth for 88.2 or 96 kHz on PCM R channel
12	Double rate audio	Optional AC-link bandwidth for 88.2 or 96 kHz on PCM C channel

The AC-link input slots dedicated to audio are defined as follows:

Slot	Name	Description
3	PCM L ADC record	16, 18, or 20-bit PCM data from left input
4	PCM R ADC record	16, 18, or 20-bit PCM data from right inputs
6	Dedicated Microphone ADC	16, 18, or 20-bit PCM data from optional 3rd ADC input
7	Vendor reserved	vendor specific (enhanced input for docking, array mic, etc)
8	Vendor reserved	vendor specific (enhanced input for docking, array mic, etc)
9	Vendor reserved	vendor specific (enhanced input for docking, array mic, etc)
12	Audio Interrupt	(or ModemGPIO) Provides optional interrupt capability for Audio Codec (not usable when a modem is present)

AC-link PCM Audio Data Format	
Bit	Description
19-4	16-bit sample (MSB bit 19, LSB bit 4)
3-0	Optional: LSBs of 18 or 20-bit sample

Table 14. Audio Slot Data Definitions

AC-link Audio Interrupt Definition	
Bit	Description
19-1	*Reserved (Audio codec will return zeros in bits 19-1)*[10]
0	Optional: Assertion = 1 will cause interrupt to be propagated to Audio controller system interrupt. See register 24h definition for enabling mechanism.[11]

Table 15. Audio Interrupt Slot Definitions

5.7 Baseline Audio Register Set

Table 16 shows the AC '97 register indexes and usage. All registers not shown and bits containing an X are assumed to be reserved.

[10] Bits 1-19 of slot 12 is dedicated to modem GPI functionality, and is declared reserved for Audio codecs. Modem usage of these slots is defined in Table 40. Slot 12-Bit Definitions) and Table 41. Recommended Slot 12 GPIO Bit Definitions).

[11] This functionality is optional for both codec and controllers. Software must ensure that both the controller and codec are capable of properly handling interrupts. In configurations where no modem capability is present, audio codecs and software could take advantage of interrupt functionality originally designed for modem features.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	na
02h	Master Volume	Mute	X	*ML5*	ML4	ML3	ML2	ML1	ML0	X	X	*MR5*	MR4	MR3	MR2	MR1	MR0	8000h
04h	*AUX Out Volume*	*Mute*	*X*	*ML5*	*ML4*	*ML3*	*ML2*	*ML1*	*ML0*	*X*	*X*	*MR5*	*MR4*	*MR3*	*MR2*	*MR1*	*MR0*	*8000h*
06h	*Mono Volume*	*Mute*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*MM5*	*MM4*	*MM3*	*MM2*	*MM1*	*MM0*	*8000h*
08h	*Master Tone*	*X*	*X*	*X*	*X*	*BA3*	*BA2*	*BA1*	*BA0*	*X*	*X*	*X*	*X*	*TR3*	*TR2*	*TR1*	*TR0*	*0F0Fh*
0Ah	*PC Beep Volume*	*Mute*	*X*	*X*	*F7*	*F6*	*F5*	*F4*	*F3*	*F2*	*F1*	*F0*	*PV3*	*PV2*	*PV1*	*PV0*	*X*	*x000h*
0Ch	*Phone Volume*	Mute	X	X	X	X	X	X	X	X	*X*	*X*	*GN4*	*GN3*	*GN2*	*GN1*	*GN0*	*8008h*
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20 dB	*X*	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	*Video Volume*	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	*X*	*X*	*GR4*	*GR3*	*GR2*	*GR1*	*GR0*	*8808h*
16h	*AUX In Volume*	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	*X*	*X*	*GR4*	*GR3*	*GR2*	*GR1*	*GR0*	*8808h*
18h	PCM Out Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
1Eh	*Record Gain Mic*	Mute	X	X	X	X	X	X	X	X	*X*	*X*	*X*	*GM3*	*GM2*	*GM1*	*GM0*	*8000h*
20h	*General Purpose*	POP	ST	3D	LD	DRSS1	DRSS0	MIX	MS	LPBK	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*0000h*
22h	*3D Control*	X	X	X	X	CR3	CR2	CR1	CR0	X	*X*	*X*	*X*	*DP3*	*DP2*	*DP1*	*DP0*	*0000h*
24h	Audio Int. & Paging	I4	I3	I2	I1	I0	X	X	X	X	X	X	X	PG3	PG2	PG1	PG0	0000h
26h	Powerdown Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	na
28h-3Ah	Extended Audio	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
3Ch-58h	Extended Modem	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	B
5Ah-5Fh	Vendor Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
60h-6Fh	Page Registers	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
70h-7Ah	Vendor Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	na
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	na

Table 16. Baseline Audio Register Map

NOTES:

1. *Italic* indicates optional feature registers or optional bits within a register. Whether implemented or not, these may be written to, but reads must return 0 if there is no support for the feature.
2. Reserved bits, marked X, can be written to but must return 0 upon read back.
3. PC_BEEP default can be 0000h or 8000h, mute off or on.

5.7.1 Reset Register (Index 00h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	na

Reading this register returns the ID code of the part and a code for the type of 3D Stereo Enhancement, if any.

Writing any value to this register performs an audio register reset, which causes all audio registers to revert to their default values. The ID defines the capabilities of AC '97 based on the following:

Bit = 1	Function
ID0	Dedicated Mic PCM In channel
ID1	Reserved (was Modem Line Codec support)
ID2	Bass & Treble control
ID3	Simulated Stereo (Mono to Stereo)
ID4	Headphone out support (not LNLVL or 4CH)
ID5	Loudness (bass boost) support
ID6	18 bit DAC resolution
ID7	20 bit DAC resolution
ID8	18 bit ADC resolution
ID9	20 bit ADC resolution

Table 17. Baseline Audio Optional Feature IDs

All DACs operate at the same resolution. All ADCs operate at the same resolution.

The standard AC '97 DAC and ADC resolutions are defined as 16-bits. 18- or 20-bit resolution implementations are optional. The audio driver for an "enhanced" AC '97 Controller can determine the implemented DAC and ADC resolution after it has been loaded by reading the AC '97 Codec's Reset Register which is located at 0x00. If, for example, the driver has determined that the implemented DAC resolution is 16-bits yet the Controller supports 18- or 20-bit sample streams for playback, the Controller can either dither the sample streams down to 16-bits or pass the stream "as is". Since all AC-link data time slots carry 20 bits, the non-dithered approach will result in the least significant bits which overrun the DAC width being dropped. For this reason dithering may be an attractive feature for the Controller that supports greater than 16-bit sample streams.

The 3D stereo enhancement decodes are based on Table 18, AC '97 48-pin package pinlist. Note that the 3D control register defines two 16-step controls for the 3D Stereo Enhancement function. These controls can be used to support center and depth, but can also be used generically. The 3D Control Register should be read to determine if the selected enhancement is either fixed or variable center and depth. If the lower 8-bits of the 3D Control Register are non-zero, then the depth/generic1 control is fixed; otherwise it is variable. If the upper 8-bits of the 3D Control Register are non-zero, then the center/generic2 control is fixed; otherwise it is variable.

SE4...SE0	3D Stereo Enhancement Technique	SE4...SE0	3D Stereo Enhancement Technique
00000 (0)	No 3D Stereo Enhancement	10000 (16)	Harman International
00001 (1)	Analog Devices	10001 (17)	Nvidia
00010 (2)	Creative Technology	10010 (18)	Philips
00011 (3)	National Semiconductor	10011 (19)	Texas Instruments
00100 (4)	Yamaha	10100 (20)	VLSI Technology
00101 (5)	BBE Sound	10101 (21)	TriTech
00110 (6)	Crystal Semiconductor	10110 (22)	Realtek
00111 (7)	Qsound Labs	10111 (23)	Samsung
01000 (8)	Spatializer Audio Laboratories	11000 (24)	Wolfson Microelectronics
01001 (9)	SRS Labs	11001 (25)	Delta Integration
01010 (10)	Platform Tech	11010 (26)	SigmaTel
01011 (11)	AKM Semiconductor	11011 (27)	KS Waves
01100 (12)	Aureal	11100 (28)	Rockwell
01101 (13)	Aztech Labs	11101 (29)	Reserved
01110 (14)	Binaura	11110 (30)	Reserved
01111 (15)	ESS Technology	11111 (31)	Reserved

Table 18. 3D Stereo Enhancement Vendor IDs

5.7.2 Play Master Volume Registers (Index 02h, 04h and 06h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	Master Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
04h	Aux Out Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
06h	Mono Volume	Mute	X	X	X	X	X	X	X	X	X	MM5	MM4	MM3	MM2	MM1	MM0	8000h

Register 02h controls the stereo master volume (both left and right channels).

Register 04h controls the optional AUX_OUT volume (AUX_OUT can be implemented as LNLVL_OUT, HP_OUT, or 4CH_OUT — see Section 5.2.1). If Aux Out Volume (Register 04h) default value (following cold or warm reset) reads 0000h, then the optional volume control is not supported. Note that the AUX_OUT may be powered down through bit PR6 in Register 26h.

Register 06h controls the optional MONO_OUT.

For all of these registers each step corresponds to 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. ML5 through ML0 is for the left channel level, MR5 through MR0 is for the right channel and MM5 through MM0 is for the mono out channel.

Support for the MSB of the level is optional. **If the MSB is not supported then AC '97 needs to detect when that bit is set and set all four LSBs to 1s.** Example: If AC '97 only supports 5 bits of resolution in its mixer and the driver writes a 1xxxxx, then AC '97 must interpret that as x11111. It will also respond when read with x11111 rather then 1xxxxx (the original value). The driver can use this feature to detect if support for the 6th bit is there or not.

The default value is 8000h (1000 0000 0000 0000), which corresponds to 0 dB attenuation with mute on.

Mute	Mx5...Mx0	Function	Range
0	00 0000	0 dB Attenuation	Req.
0	01 1111	46.5 dB Attenuation	Req.
0	11 1111	94.5 dB Attenuation	Optional
1	xx xxxx	∞ dB Attenuation	Req.

Table 19. Master, Aux Out, and Mono Volume

5.7.3 Master Tone Control Registers (Index 08h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
08h	Master Tone	X	X	X	X	BA3	BA2	BA1	BA0	X	X	X	X	TR3	TR2	TR1	TR0	0F0Fh

Optional register for support of tone controls (bass and treble). If the part does not support bass and treble, writing to this register will have no effect and reading will result in all zeroes. The step size is 3 dB with optional support for 1.5 dB. The step size option is accomplished by either using 3 bits (MSB justified) for 3 dB steps or all 4 bits for 1.5 dB steps. Writing a 0000h corresponds to +10.5 dB of gain. Center frequencies (from which gains are measured) are 100 Hz for Bass and 10 kHz for Treble. The default value is 0F0Fh, which corresponds to bypass of bass or treble gain.

TR3...*TR0* or BA3...*BA0*	Support Required	Function
000*0*	yes	+10.5 dB of gain
000*1*	no	+9 dB of gain
001*0*	yes	+7.5 dB of gain
001*1*	no	+6 dB of gain
..		...
011*0*	yes	+1.5 dB of gain
011*1*	yes	0 dB of gain
100*0*	yes	-1.5 dB of gain
..		...
110*0*	yes	-7.5 dB
110*1*	no	-9 dB of gain
111*0*	yes	-10.5 dB of gain
111*1*	yes	Bypass

Table 20. Tone Control

5.7.4 PC Beep Register (Index 0Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ah	*PC Beep Volume*	*Mute*	*X*	*X*	*F7*	*F6*	*F5*	*F4*	*F3*	*F2*	*F1*	*F0*	*PV3*	*PV2*	*PV1*	*PV0*	*X*	*x000h*

This controls the level and frequency for the optional PC Beep.

PV3-PV0 controls the volume of the input signal, if implemented, and the generated signal, if implemented. Each step corresponds to approximately 3 dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB.

If F7-F0 are writeable, then the optional PCBEEP generation is supported. The beep frequency generated is the result of dividing the 48kHz48KHz clock by 4 times the number specified in F[7:0], allowing tones from 47 Hz to 12kHz. A value of 00h in bits F[7:0] disables internal PC Beep generation and enables the external PC Beep input if available. The PV bits control the volume level of the generated signal. The generated signal is not intended to be a high quality sine wave. The clock output rounded with a capacitor provides sufficient signal quality to provide beep code signaling.

The PC_BEEP input supports motherboard AC '97 Controller /Codec implementations. The intention of routing PC_BEEP through the Codec analog mixer is to eliminate the requirement for an onboard speaker or piezoelectric device by ensuring a connection to speakers connected via the output jack. In order for this to be viable the PC_BEEP signal needs to reach the output jack at all times, with or without the audio driver's support. PC_BEEP frequency generation supports for motherboard and riser implementations, as no signal needs to be routed.

NOTE: It is recommended that the PC_BEEP be routed to L & R Line outputs even when AC '97 is in a RESET State. This is so that Power On Self Test (POST) codes can be heard by the user in case of a hardware problem with the PC. This can be accomplished with a high impedance path to the outputs without any attenuation.

The default value can be 0000h or 8000h, which corresponds to 0 dB attenuation with mute off or on.

Mute	PV3...PV0	Function
0	0000	0 dB Attenuation
0	1111	45 dB Attenuation
1	xxxx	∞ dB Attenuation

Table 21. PC BEEP Volume

5.7.5 Analog Mixer Input Gain Registers (Index 0Ch - 18h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ch	*Phone Volume*	*Mute*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*GN4*	*GN3*	*GN2*	*GN1*	*GN0*	*8008h*
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20 dB	*X*	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	*Video Volume*	*Mute*	*X*	*X*	*GL4*	*GL3*	*GL2*	*GL1*	*GL0*	*X*	*X*	*X*	*GR4*	*GR3*	*GR2*	*GR1*	*GR0*	*8808h*
16h	*Aux In Volume*	*Mute*	*X*	*X*	*GL4*	*GL3*	*GL2*	*GL1*	*GL0*	*X*	*X*	*X*	*GR4*	*GR3*	*GR2*	*GR1*	*GR0*	*8808h*
18h	PCM Out Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h

This controls the gain/attenuation for each of the analog inputs. Each step corresponds to approximately 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB.

- **Register 0Eh** (Mic Volume Register) has an extra bit that is for a 20 dB boost. When bit 6 is set to 1 the 20 dB boost is on. The default value is 8008, which corresponds to 0 dB gain with mute on.

The default value for the mono registers is 8008h, which corresponds to 0 dB gain with mute on. The default value for stereo registers is 8808h, which corresponds to 0 dB gain with mute on.

Mute	Gx4...Gx0	Function
0	00000	+12 dB gain
0	01000	0 dB gain
0	11111	-34.5 dB gain
1	xxxxx	–∞ dB gain

Table 22. Mixer Input Gain/Atten

5.7.6 Record Select Control Register (Index 1Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h

This register is used to select the record source independently for right and left. See table for legend. Several of the analog mixer inputs are optional, selecting an unimplemented analog input has undefined results.

The default value is 0000h, which corresponds to Mic in.

SR2...SR0	Right Record Source
0	Mic
1	CD In (R)
2	Video In (R)
3	Aux In (R)
4	Line In (R)
5	Stereo Mix (R)
6	Mono Mix
7	Phone

SL2...SL0	Left Record Source
0	Mic
1	CD In (L)
2	Video In (L)
3	Aux In (L)
4	Line In (L)
5	Stereo Mix (L)
6	Mono Mix
7	Phone

Table 23. Left, Right Record Select

5.7.7 Record Gain Registers (Index 1Ch and 1Eh)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
1Eh	Record Gain Mic	Mute	X	X	X	X	X	X	X	X	X	X	X	GM3	GM2	GM1	GM0	8000h

1Ch is for the stereo input and 1Eh is for the optional dedicated mic channel. Each step corresponds to 1.5 dB. 22.5dB corresponds to 0F0Fh and 000Fh respectively. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel(s) is set at -∞ dB.

The default value is 8000h, which corresponds to 0 dB gain with mute on.

Mute	Gx3...Gx0	Function
0	1111	+22.5 dB gain
0	0000	0 dB gain
1	xxxxx	–∞ dB gain

Table 24. Record Gain/Attenuation

5.7.8 General Purpose Register (Index 20h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	General Purpose	POP	ST	3D	LD	DRSS1	DRSS0	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h

This register is used to control miscellaneous optional functions of the AC '97 component. Below is a summary of each bit and its function. The *POP* bit controls the optional PCM out 3D bypass path (the pre- and post-3D PCM out paths are mutually exclusive). The *MS* bit controls the optional microphone selector. The Loudness (bass boost) bit is to control an optional loudness contour or "bass boost" function. The exact implementation of this is left up to the vendor. The optional DRSS[1:0] bits control which slots the *n+1* data is present on for Double Rate Audio. This register should be read before writing to generate a mask for only the bit(s) that need to be changed. The function default value is 0000h (all bits are off). The optional LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements.

Bit	Function
POP	PCM out path & mute, 0 = pre 3D, 1 = post 3D
ST	Simulated Stereo Enhancement on/off 1 = on
3D	3D Stereo Enhancement on/off 1 = on
LD	Loudness (bass boost) on/off 1 = on
DRSS[1:0]	Double Rate Slot Select 00: PCM L, R, C n+1 data is on Slots 10-12 (default) 01: PCM L, R n+1 data is on slots 7, 8 10: Reserved 11: Reserved
MIX	Mono output select 0=Mix, 1=Mic
MS	Mic select 0 = Mic1, 1= Mic2
LPBK	ADC/DAC loopback mode

Table 25. General Purpose Bit Definitions

5.7.9 3D Control Register (Index 22h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
22h	3D Control	X	X	X	X	CR3	CR2	CR1	CR0	X	X	X	X	DP3	DP2	DP1	DP0	0000h

This optional register is used to control the center and/or depth of the 3D stereo enhancement function built into the AC '97 component. Note this register should be read to indicate if the selected 3D stereo enhancement is of either fixed or variable center and depth. If this control register is non-zero then the enhancement is fixed. The register default value is either the fixed value or 0000h if it is variable. Linear or logarithmic implementation is acceptable, depending on the 3D technology (linear is shown below):

CR3...CR0 DP3...DP0	Center Depth
0	0%
1	6.67%
.	.
14	93.33%
15	100%

Table 26. 3D Control

5.7.10 Audio Interrupt and Paging Mechanism (Index 24h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
24h	Audio Int. & Paging	I4	I3	I2	I1	I0	X	X	X	X	X	X	X	PG3	PG2	PG1	PG0	X

This register was originally (AC '97 1.03) modem sample rate, later reserved (AC '97 2.0). It is redefined to support Audio interrupt and register paging mechanism.

Bit	Default	Function
I4	0	Interrupt Status (R/W) 0 - Interrupt is clear 1 - Interrupt was generated Interrupt event is cleared by writing a 1 to this bit. The interrupt bit will change regardless of condition of interrupt enable (I0) status. An interrupt in the GPI in slot 12 in the AC link will follow this bit change when interrupt enable (I0) is un-masked. If this bit is set, one or both of I3 or I2 must be set to indicate the interrupt cause.
I[3:2]	00	Interrupt Cause (RO) I [2]= 0 - Sense status has not changed (did not cause interrupt) (default) 1 - Sense cycle completed or new sense information is available. I [3]= 0 - GPIO status change did not cause interrupt (default) 1 - GPIO status change caused interrupt. These bits will indicate the cause(s) of an interrupt. This information should be used to service the correct interrupting event(s). If the Interrupt Status (bit I4) is set, one or both of these bits must be set to indicate the interrupt cause. Hardware must reset these bits back to zero when the Interrupt Status bit is cleared.
I1	0	Sense Cycle (RW) 0 - Sense cycle not in progress 1 - Sense cycle start Writing a 1 to this bit causes a sense cycle start if supported. If sense cycle is not supported this bit is RO. If a sense cycle is in progress, writing a '0' to this bit will abort the sense cycle. The data in the sense result register (6Ah) may or may not be valid, as determined by the IV bit.
I0	0	Interrupt Enable (RW) 0 - Interrupt generation is masked 1 - Interrupt generation is un-masked S/W should Not un-mask the interrupt unless ensured by the AC '97 controller that no conflict is possible with modem slot 12- GPI functionality. AC '97 2.2 compliant controllers will not likely support audio codec interrupt infrastructure. In that case, s/w could poll the interrupt status after initiating a sense cycle and waiting for Sense Cycle Max Delay to determine if an interrupting event has occurred.
X	X	Reserved
PG[3:0]	0h	Page Selector (RW): 0h - Vendor Specific 1h – Page ID 01(see correspondent definition section 5.8.7) 2h-Fh – Reserved Pages This register is used to select a descriptor of 16 word pages between registers 60h to 6Fh. A value of 0h is used to select vendor specific space to maintain compatibility with AC '97 2.2 vendor specific registers. System software can determine implemented pages by writing the page number and reading the value back. If the value read back does not match the value written, the page is not implemented. All implemented pages must be in consecutive. (i.e., page 2h cannot be implemented without page 1h)

Table 27. Audio Interrupt and Paging Mechanism bits definition

5.7.11 Powerdown Control/Status Register (Index 26h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
26h	Powerdown Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	na

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status, with a 1 indicating that the subsection is "ready". Ready is defined as the subsection able to perform in its nominal state. When this register is written the bit values that come in on AC-link will have no effect on read only bits 0-7.

When the AC-link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1 it indicates that the AC-link and AC '97 Control and Status Registers are in a fully operational state. The AC '97 Controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any, are ready.

Bit	Function
X	Reserved
REF	Vref's up to nominal level
ANL	Analog mixers, etc. ready
DAC	DAC section ready to accept data
ADC	ADC section ready to transmit data

Table 28. Baseline Powerdown Status bit Definitions

The powerdown modes are as follows. The first three bits are to be used individually rather than in combination with each other. PR3 can be used in combination with PR2 or by itself. PR0 and PR1 control the PCM ADCs and DACs only.

Bit	Function
PR0	PCM in ADC's & Input Mux powerdown
PR1	PCM out DACs powerdown
PR2	Analog Mixer powerdown (Vref still on)
PR3	Analog Mixer powerdown (Vref off)
PR4	Digital Interface (AC-link) powerdown (external clk off)
PR5	Internal Clk disable
PR6	Aux out powerdown
EAPD	External Amplifier powerdown

Table 29. Baseline Powerdown Control bit Definitions

EAPD (formerly PR7) independently controls an output pin that manages an optional external audio amplifier. AC '97 compliance requires the implementation of a dedicated output pin for external audio amplifier control. The pin is controlled via the "EAPD" (External Amplifier Powerdown) bit in Powerdown Ctrl/Stat Register 26h, bit 15 (formerly PR7). EAPD = 0 places a 0 on the output pin, enabling an external audio amplifier, EAPD = 1 shuts it down. Audio amplifier devices that operate with reverse polarity may require an external inverter. The pin assignment is pin 47 on the 48-pin QFP package. The list of pins that are disabled in ATE test mode should include the external amplifier powerdown output pin.

Power-up default is EAPD = 0 (external audio amplifier enabled).

5.8 Extended Audio Register Set

The extended audio registers support variable sample rate audio output and input, double-rate audio output, multichannel audio output, and S/PDIF output.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	ID1	ID0	x	x	REV1	REV0	AMAP	LDAC	SDAC	CDAC	DSA1	DSA0	VRM	SPDIF	DRA	VRA	xxxxh
2Ah	Ext'd Audio Stat/Ctrl	VCFG	PRL	PRK	PRJ	PRI	SPCV	MADC	LDAC	SDAC	CDAC	SPSA1	SPSA0	VRM	SPDIF	DRA	VRA	xxxxh
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
2Eh	PCM Surr DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
30h	PCM LFE DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM L/R ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
34h	Mic ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
36h	Center/LFE Volume	Mute	x	LFE5	LFE4	LFE3	LFE2	LFE1	LFE0	Mute	x	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0	8080h
38h	Surr Volume	Mute	x	LSR5	LSR4	LSR3	LSR2	LSR1	LSR0	Mute	x	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0	8080h
3Ah	S/PDIF Control	V	DRS	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/AUDIO	PRO	2000h

Table 30. AC '97 Extended Audio Register Set

5.8.1 Extended Audio ID Register (Index 28h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	ID1	ID0	x	x	REV1	REV0	AMAP	LDAC	SDAC	CDAC	DSA1	DSA0	VRM	SPDIF	DRA	VRA	xxxxh

The Extended Audio ID is a read only register (except for the new bits D5 and D4, which are read/write) that identifies which extended audio features are supported (in addition to the original AC '97 features identified by reading the Reset Register at Index 00h). A non-zero Extended Audio ID value indicates one or more of the extended audio features are supported.

- VRA=1 indicates optional Variable Rate PCM Audio is supported
- DRA=1 indicates optional Double-Rate PCM Audio output is supported
- SPDIF=1 indicates optional S/PDIF transmitter is supported. S/PDIF PCM is defined in IEC958 (IEC60958), encoded multichannel (AC-3, MPEG, DTS, etc.) is defined in IEC61937. The recently published Amendment 1 to IEC60958-3 contains a proposal for higher sample rate support.
- VRM=1 indicates optional Variable Rate MIC input is supported
- DSA[1,0] are read/write bits that control optional DAC Slot Assignment as described in Table 32
- CDAC=1 indicates optional PCM Center DAC is supported
- SDAC=1 indicates optional PCM Surround L&R DACs are supported
- LDAC=1 indicates optional PCM LFE DAC is supported
- AMAP=1 indicates support for slot/DAC mappings based on Codec ID
- REV[1:0]=10 indicates Codec is AC '97 revision 2.3 compliant. Codec compliant to older revisions will have REV[1:0] set as indicated in Table 31 AC'97 Revision ID.

REV1, REV0	AC'97 Revision
00	Revision 2.1 or earlier
01	Revision 2.2
10	Revision 2.3
11	Reserved

Table 31 AC'97 Revision ID

- ID1, ID0 is a 2-bit field which indicates the Codec configuration: Primary is 00; Secondary is 01, 10, or 11

DSA1, DSA0	DACs 1,2	DACs 3,4	DACs 5,6
00	slots 3&4	slots 7&8	slots 6&9
01	7&8	6&9	10&11
10	6&9	10&11	3&4
11	10&11	3&4	7&8

Table 32 Optional DAC Slot duty

If optional Variable Rate Audio is supported by the Codec, the AC '97 Controller can further identify the specific capabilities of each DAC/ADC group by enabling VRA mode (VRA=1 in the Extended Audio Status and Control Register) and writing and reading values to/from the associated Sample Rate Control Registers (defined below).

The value after cold or register reset for this register is constant, and depends on the features supported and the hardware configuration as Primary or Secondary Codec.

5.8.2 Extended Audio Status and Control Register (Index 2Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ah	Ext'd Audio Stat/Ctrl	VCFG	PRL	PRK	PRJ	PRI	SPCV	MADC	LDAC	SDAC	CDAC	SPSA1	SPSA0	VRM	SPDIF	DRA	VRA	xxxxh

The Extended Audio Status and Control Register is a read/write register that provides status and control of the extended audio features.

Bits D3-D0 are read/write controls that enable or disable the extended audio features

- VRA=1 enables Variable Rate Audio mode (VRA uses sample rate control Registers 2C-32h). Upon reset, the audio sample rate registers default to 48 kHz, and VRA=0. When VRA is set to 0 the registers are forced to BB80h (48 kHz) because that is the only rate supported, and any values previously written to these registers are lost. Note that modem converters (line1, line2, handset) are not affected by the VRA bit, and SLOTREQ bits for active modem DACs are always treated as valid (data on demand).
- DRA=1 enables Double-Rate Audio mode in which data from PCM L and PCM R in output slots 3 and 4 is used in conjunction with PCM L (n+1) and PCM R (n+1) data, to provide DAC streams at twice the sample rate designated by the PCM Front Sample Rate Control Register. Note that DRA can be used without VRA; in that case the converter rates are forced to 96 kHz if DRA=1. The slots on which the (n+1) data is transmitted on is indicated by the DRSS[1:0] bits in the General Purpose register 20h.
- SPDIF=1 enables the S/PDIF transmitter, SPDIF defaults to transmitter subsystem off (powerdown)
- VRM=1 enables Variable Rate Audio mode for the dedicated MIC ADC (VRM uses sample rate Register 34h). VRM controls the optional Mic ADC behavior in the same way that VRA controls the PCM ADC.

Bits D5-D4, SPSA[1:0], are read/write bits that control the S/PDIF AC-link Slot Assignment. Support for slots 3&4, 7&8, and 6&9 is required, and 10&11 is also recommended. The Controller or driver must perform write followed by read to determine if support for optional slots 10&11 is implemented. All S/PDIF capable Primary Codecs must support the following programming assignments, with the default S/PDIF slot assignment corresponding to the first non-dedicated AC-link slot pair depending on the number of DAC channels supported.

- SPSA[1,0] = 00 S/PDIF source data assigned to AC-link slots 3&4
- SPSA[1,0] = 01 S/PDIF source data assigned to AC-link slots 7&8 [2-ch Primary Codec default]
- SPSA[1,0] = 10 S/PDIF source data assigned to AC-link slots 6&9 [4-ch Primary Codec default]
- SPSA[1,0] = 11 S/PDIF source data assigned to AC-link slots 10&11 [6-ch Primary Codec default]

AMAP compliance is a requirement for AC ’97 2.2 Controllers and Codecs. AMAP compliant Codecs must support the above programming assignments — only the default SPSA value changes according to Codec ID mapping, as shown in Table 33:

Codec ID	Function	SPSA = 00	SPSA = 01	SPSA = 10	SPSA = 11
00	2-ch Primary w/ S/PDIF	3&4	7&8 [default]	6&9	10&11
00	4-ch Primary w/ S/PDIF	3&4	7&8	6&9 [default]	10&11
00	6-ch Primary w/ S/PDIF	3&4	7&8	6&9	10&11 [default]
01	+2-ch Secondary w/ S/PDIF	3&4	7&8	6&9 [default]	
01	+4-ch Secondary w/ S/PDIF	3&4	7&8	6&9	10&11 [default]
10	+2-ch Secondary w/ S/PDIF	3&4	7&8	6&9 [default]	
10	+4-ch Secondary w/ S/PDIF	3&4	7&8	6&9	10&11 [default]
11	+2-ch Secondary w/ S/PDIF	3&4	7&8	6&9	10&11 [default]

Table 33. AC ‘97 2.2 AMAP Compliant Default S/PDIF Slot Assignments

Bits D9-D6 are read only status of the extended audio feature readiness

- CDAC=1 indicates the PCM Center DAC is ready (multichannel Codecs)
- SDAC=1 indicates the PCM Surround DACs are ready (multichannel Codecs)
- LDAC=1 indicates the PCM LFE DAC is ready (multichannel Codecs)
- MADC=1 indicates the MIC ADC is ready (new status for previously-defined AC ‘97 feature)

Bit 10, SPCV, (S/PDIF Configuration Valid), is a read only bit that indicates the status of the S/PDIF transmitter subsystem, enabling the driver to determine if the currently programmed S/PDIF configuration is supported. SPCV is always valid, independent of the SPDIF enable bit status.

- SPCV =0 indicates current S/PDIF configuration {SPSA, SPSR, DAC/slot rate, DRS} is not valid (not supported)
- SPCV =1 indicates current S/PDIF configuration {SPSA, SPSR, DAC/slot rate, DRS} is valid (is supported)

Bits D14-D11 are read/write controls of the extended audio feature powerdown

- PRI=1 turns the PCM Center DAC off (multichannel Codecs)
- PRJ=1 turns the PCM Surround DACs off (multichannel Codecs)
- PRK=1 turns the PCM LFE DACs off (multichannel Codecs)
- PRL=1 turns the MIC ADC off (MIC ADC operation is independent of PR0 from 26h)

The default value after cold or register reset for this register is all extended features disabled (D3-D0 =0) and powered down (D14-D11=1). The feature readiness status should always be accurate (D10-D6=x).

Bit D15, VCFG, determines S/P-DIF transmitter behavior when data is not being transmitted. When asserted, this bit forces the de-assertion of the S/PDIF “Validity” flag, which is bit 28 transmitted in each S/PDIF sub-frame. The AC ’97 ‘V’ bit is defined in the S/P-DIF Control Register 3Ah.

- If "V" = 0 and “VCFG”=0, then for each S/PDIF sub-frame (Left & Right), bit<28> "Validity” flag reflects whether or not an internal Codec error has occurred (specifically whether the S/PDIF interface received and transmitted a valid sample from the AC-Link). If a valid sample (Left or Right) was received and successfully transmitted, the "Validity” flag should be "0" for that sub-frame. Otherwise, the "Validity” flag for that sub-frame should be transmitted as "1".
- If “V”=0 and “VCFG” = 1, then for each S/PDIF sub-frame (Left & Right), bit<28> "Validity” flag reflects whether or not an internal CODEC transmission error has occurred. Specifically an internal CODEC error

should result in the "Validity" flag being set to "1". In the case where the S/PDIF transmitter does is not receiving a sample or does not receive a valid sample from the AC'97 controller, (Left or Right), the S/PDIF transmitter should set the S/PDIF "Validity" flag to "0" and pad each of the S/PDIF "Audio Sample Word" in question with "0"s for the sub-frame in question. If a valid sample (Left or Right) was received and successfully transmitted, the "Validity" flag should be "0" for that sub-frame.

- If "V"=1 and "VCFG" = 0, then each S/PDIF subframe (Left & Right) should have bit<28> "Validity" flag = 1. This tags all S/PDIF sub-frames as invalid.
- "V"=1 and "VCFG"=1 state is reserved for future use.
- Default state, coming out of reset, for "V" and "VCFG" should be 0 and 0 respectively.

5.8.3 Audio Sample Rate Control Registers (Index 2Ch – 34h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ch	PCM Front DAC Rate (output slots 3, 4, 6)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
2Eh	PCM Surr DAC Rate (output slots 7, 8)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
30h	PCM LFE DAC Rate (output slot 9)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM L/R ADC Rate (input slots 3, 4)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
34h	Mic ADC Rate (input slot 6)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

In Variable Rate Audio (VRA) or Mic (VRM) modes, DACs and ADCs are governed by read/write sample rate control registers that contain 16-bit unsigned values between 0 and 65535, representing the rate of operation in Hz. DAC and ADC groups should be capable of operating at independent rates, otherwise a currently active DAC or ADC rate may limit availability of the associated converter.

In both VRA and VRM modes, if the value written to the register is supported that value will be echoed back when read, otherwise the closest (higher in case of a tie) sample rate supported is returned.

In Double Rate Audio (DRA) mode, the programmed audio DAC sample rates programmed are multiplied by 2x. As an example: For 88.2 kHz DAC operation, the sample rate programmed would be 44.1 kHz, and the DRA bit will be programmed to 1. DRA does NOT affect input ADC operation.

Variable Rate Audio is essential to low cost integrated audio solutions — the minimum requirement is dual-rate operation at either 44.1 or 48 kHz, with additional support for 8.0, 11.025, 16, 22.05, and 32 kHz recommended.

The default value after cold or register reset for the audio sample rate control registers is BB80h (48 kHz) and VRA=0. When VRA is set to 0 the registers are forced to BB80h (48 kHz) because that is the only rate supported, and any values previously written to these registers are lost.

5.8.4 Surround and Center/LFE Volume Control Registers (Index 36h and 38h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
36h	Center/LFE Volume	Mute	x	LFE5	LFE4	LFE3	LFE2	LFE1	LFE0	Mute	x	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0	8080h
38h	Surround Volume	Mute	x	LSR5	LSR4	LSR3	LSR2	LSR1	LSR0	Mute	x	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0	8080h

These read/write registers control the output volume of the optional four PCM channels, and applies to monolithic multichannel Codecs. Values written to the fields behave the same as the Play Master Volume Register (Index 02h), which offers attenuation but no gain. There is an independent mute (1=on) for each channel.

The default value after cold or register reset for this register (8080h) corresponds to 0 dB attenuation with mute on.

5.8.5 S/PDIF Control Register (Index 3Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Ah	S/PDIF Control	V	DRS	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/AUDIO	PRO	2000h

Register 3Ah is a read/write register that controls S/PDIF functionality and manages bit fields propagated as channel status (or subframe in the V case). With the exception of V, this register should only be written to when the S/PDIF transmitter is disabled (SPDIF bit in Register 2Ah is "0"). This ensures that control and status information start up correctly at the beginning of S/PDIF transmission.

V Validity: This bit affects the "Validity flag", bit<28> transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. The behavior of the S/PDIF transmitter with respect to this bit depends on the value of the VCFG bit in the Extended Audio Status and Control register. The behavior of the transmitter is defined in the definition of the Extended Audio Status and Control Register (Index 2Ah), section 5.8.2.

DRS Double Rate S/PDIF: This bit controls support for optional higher sample rate transmission. When DRS is enabled "1" and SPSA is configured {"01", "10", or "11"} the S/PDIF transmitter uses AC-link slots 3&4 + {7&8, 6&9, or 10&11} to supply data at Fs = 64, 88.2 or 96 kHz. The SPCV bit must indicate a valid configuration. A DRS capable Codec must automatically determine the correct channel status bits for Fs from DRS and SPSR and insert them as necessary. The Controller or Driver must perform write followed by read to determine if DRS is supported.

SPSR[1,0] S/PDIF Sample Rate: This field controls the S/PDIF transmitter clock rate (64*Fs unless DRS is enabled). The Controller or Driver must perform write followed by read to determine if the optional 32 and 44.1 kHz rates are supported.

- SPSR[1:0] = "00", sample rate set to 44.1kHz (optional)
- SPSR[1:0] = "01", reserved
- SPSR[1:0] = "10", sample rate set to 48 kHz [default]
- SPSR[1:0] = "11", sample rate set to 32 kHz (optional)

L Generation Level: programmed according to IEC standards, or as appropriate

CC[6-0] Category Code: programmed according to IEC standards, or as appropriate

PRE Preemphasis: "1" indicates filter preemphasis is 50/15 µsec, "0" preemphasis is none.

COPY Copyright: "1" indicates copyright is asserted, "0" copyright is not asserted.

/AUDIO Non-Audio: "1" indicates data is non PCM format, "0" data is PCM.

PRO Professional: "1" indicates Professional use of channel status, "0" Consumer.

5.8.6 Vendor Reserved Registers (Index 5Ah - 5Fh, 70h - 7Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
5Ah-5Fh, 70hh-7Ah	Vendor Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

These are reserved for vendor specific use. Driver writers should not access these registers unless the Vendor ID register has been checked first to ensure that the vendor of the AC '97 component has been identified.

5.8.7 Extended Codec Registers Page Structure Definition

Reg	PG ID	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
60h-6Eh	01h	Register Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	na

Bit	Default	Function
D[15:0]	na	Extended Codec Registers Bits: These register allow for the definition of further capabilities from those found in previous AC '97 definitions.

Table 34. Extended Codec Registers bits definition

These bits provide a paged address space for extended codec information. The Page Selector bits in the Audio Interrupt and Paging register (Register 24h bits 3:0) control the page of information viewed through this page window.

5.8.7.1 Extended Registers Page 00

Page 00 of the Extended Codec Registers is reserved for vendor specific use. Driver writers should not access these registers unless the Vendor ID register has been checked first to ensure that the vendor of the AC '97 component has been identified and the usage of the vendor defined registers is understood.

5.8.7.2 Extended Registers Page 01

The usage Page 01 of the Extended Codec Registers is defined in section 5.9.

5.8.7.3 Extended Registers Page 02-0Fh

Pages 02 through 0Fh of the Extended Codec Registers are reserved for future use, and are not to be used by codec hardware vendors or driver writers.

5.8.8 Vendor ID Registers (Index 7Ch - 7Eh)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	na
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0	na

All AC '97 Codecs are required to implement specific vendor identification, and this is essential for riser card identification. The ID method is Microsoft's Plug and Play Vendor ID code with F7..0 being the first character of that ID, S7..0 being the second character and T7..0 the third character. These three characters are ASCII encoded. The DEV[7:0] field allows for a vendor specific Device ID number for the specific codec.

5.9 Extended Codec Registers Page '01'

The Extended Codec Registers Page '01' implements an extended set of registers for identification and control of the codec. The Codec Class/Rev, PCI SVID, PCI SID registers provide extended information to identify the specific codec hardware and surrounding support hardware. The Function Select, Function Information, and Senses Details registers provide information to determine the connected peripherals and support hardware. The DAC and ADC slot mapping registers allow significantly more flexibility in the configuration of the codec by allowing DACs or ADCs to decode arbitrary link data slots.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
60h	Codec Class/Rev	X	X	X	CL4	CL3	CL2	CL1	CL0	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0	na
62h	PCI SVID	PVI15	PVI14	PVI13	PVI12	PVI11	PVI10	PVI9	PVI8	PVI7	PVI6	PVI5	PVI4	PVI3	PVI2	PVI1	PVI0	na
64h	PCI SID	PI15	PI14	PI13	PI12	PI11	PI10	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	na
66h	Function Select	X	X	X	X	X	X	X	X	X	X	X	FC3	FC2	FC1	FC0	T/R	0h
68h	Function Information	G4	G3	G21	G1	G0	INV	DL4	DL3	DL2	DL1	DL0	IV	X	X	X	FIP	na
6Ah	Sense details	ST2	ST1	ST0	S4	S3	S2	S1	S0	OR1	OR0	SR5	SR4	SR3	SR2	SR1	SR0	na
6Ch	DAC Slot Mapping	FD3	FD2	FD1	FD0	SD3	SD2	SD1	SD0	CLD3	CLD2	CLD1	CLD0	X	X	X	X	3760h
6Eh	ADC Slot Mapping	LIA3	LIA2	LIA1	LIA0	IMA3	IMA2	IMA1	IMA0	X	X	X	X	X	X	X	MV	3600h

Table 35. Extended Codec Register Set

5.9.1 Discovery Descriptor Definition

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
60h	Codec Class/Rev	X	X	X	CL4	CL3	CL2	CL1	CL0	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0	na
62h	PCI SVID	PVI15	PVI14	PVI13	PVI12	PVI11	PVI10	PVI9	PVI8	PVI7	PVI6	PVI5	PVI4	PVI3	PVI2	PVI1	PVI0	na
64h	PCI SID	PI15	PI14	PI13	PI12	PI11	PI10	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	na

The Discovery Descriptor Definition provides information to identify the hardware by providing a PCI SVID and SID, and providing revision and programming class information. This information is supplemental to the codec information in the Vendor ID Registers (7Ch and 7Eh).

Bit	Default	Function
RV[7:0]	na	Revision ID: (RO) This register specifies a device specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. This field should be viewed as a vendor defined extension to the codec ID. This number changes with new codec stepping of the same codec ID.
CL[4:0]	na	Codec Compatibility Class (RO) This is a codec vendor specific field to define s/w compatibility for the codec. S/W read this field together with codec vendor ID (reg 7C-7Eh) to determine vendor specific programming interface compatibility. S/w can rely on vendor specific register behavior to be compatible among vendor codecs of the same class. 00h – Field not implemented 01h-1Fh – Vendor specific compatibility class code
X	0h	Reserved
PVI[15:0]	na	PCI Sub System Vendor ID: (Optional) This field provides the PCI Sub System Vendor ID of the Audio or Modem Sub Assembly Vendor (i.e., CNR manufacturer, Motherboard Vendor). This is NOT the codec vendor PCI Vendor ID, nor is it the AC '97 controller PCI Vendor ID. If not implemented this register is read only and must return value of 0x0h when read. If the register is implemented and data is not available it should return FFFFh.
PI[15:0]	na	PCI Vendor ID: (Optional) This field provides the PCI Sub System ID of the Audio or Modem Sub Assembly (i.e., CNR Model, Motherboard SKU). This is NOT the codec vendor PCI ID, nor is it the AC '97 controller PCI ID. Information in this field must be available for AC '97 controller reads when codec ready is asserted in AC link. If not implemented this register is read only and must return value of 0x0h when read. If the register is implemented and data is not available it should return FFFFh.

Table 36. Discovery Register bits definition

5.9.2 Audio Input/Output Capabilities Register

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
66h	Function Select	X	X	X	X	X	X	X	X	X	X	X	FC3	FC2	FC1	FC0	T/R	0h
68h	Function Information	G4	G3	G2	G1	G0	INV	DL4	DL3	DL2	DL1	DL0	IV	X	X	X	FIP	na
6Ah	Sense details	ST2	ST1	ST0	S4	S3	S2	S1	S0	OR1	OR0	SR5	SR4	SR3	SR2	SR1	SR0	na

Table 37. Audio Input/Output Capabilities Page ID 01

5.9.2.1 Function Select Register (Index 66h)

Bit	Default	Function
FC[3:0]	0h	Function Code bits These bits specify the type of audio function described by this page. The codec must provide information in this register. 00h – DAC 1 (Master Out) 01h – DAC 2 (AUX Out) 02h – DAC 3 (C/LFE) 03h - S/P-DIF out 04h – Phone In 05h – Mic 1 (Mic Select = 0) 06h – Mic 2 (Mic Select = 1) 07h – Line In 08h – CD In 09h – Video In 0Ah – Aux In 0Bh – Mono out 0C - 0Fh – Reserved These bits are Read/Write and represent current AC '97 2.2 defined I/O capabilities. S/W will program the corresponding I/O number in this field together with the Ring/Tip selector bit below T/R. Once S/W program the value and properly read it back to confirm selection and implementation, it will access the rest of the bits fields in the descriptor. A read-only value of zero in this register, along with a read only value of zero in the IV bit, indicates that the codec does not support the Information and I/O register.
T/R	0	Tip or Ring selection Bit. This bit sets which jack conductor the sense value is measured from. S/W will program the corresponding the Ring/Tip selector bit together with the I/O number in bits FC[3:0]. Once S/W program the value and properly read it back to confirm selection and implementation, it will access the rest of the bits fields in the descriptor. 0 – Tip 1 – Ring Mono inputs and outputs should report the relevant Function and Sense information when T/R is set to '0' (Tip). The FIP bit should report '0' (Page 01h, register 68h, bit 0 reports No Function Information Present) when T/R is set to a '1' on a mono input or output.

5.9.2.2 Information and I/O Register (Index 68h)

<table>
<tr><th>Bit</th><th>Default</th><th>Function</th></tr>
<tr><td>G4</td><td>Codec default</td><td>Gain Sign Bit

The codec updates this bit with the sign of the gain value present in G[3:0]. The BIOS updates this to take into consideration external amplifiers or other external logic when relevant.</td></tr>
<tr><td>G[4:0]</td><td>Codec default</td><td>Gain bits

The codec updates these bits with the gain value (dB relative to level-out) in 1.5dBV increments. The BIOS updates these to take into consideration external amplifiers or other external logic when relevant.

G[3:0] indicates the magnitude of the gain. G[4] indicates whether the value is a gain or attenuation.

<table><tr><td>G[4:0]</td><td>Gain or Attenuation (dB relative to level-out)</td></tr><tr><td>00000</td><td>0 dBV</td></tr><tr><td>00001</td><td>1.5 dBV</td></tr><tr><td>01111</td><td>24 dBV</td></tr><tr><td>10001</td><td>-1.5 dBV</td></tr><tr><td>11111</td><td>-24 dBV</td></tr></table>
These bits are read/write</td></tr>
<tr><td>INV</td><td>Codec default</td><td>Inversion bit

Indicates that the codec presents a 180 degree phase shift to the signal.

0h – No inversion reported

1h – Inverted

The Inv bit is Read/Write.</td></tr>
<tr><td>DL[4:0]</td><td>Codec default</td><td>Buffer delays:

Codec will provide number a value that represents the delay measurement for the input and output channels. Software will use this value to accurately calculate audio stream position with respect to what is been reproduced or recorded.

These values are in 20.83 microsecond (1/48000 second) units.

For output channels, this timing is from the end of AC Link frame in which the sample is provided, until the time the analog signal appears at the output pin.

For input streams, this is from when the analog signal is presented at the pin until the representative sample is provided on the AC Link. Analog to Analog paths are not considered in this measurement.

The measurement is a 'typical' measurement, at a 48KHz sample rate, with minimal in-codec processing (i.e., 3D effects are turned off.)

00h – Information not provided

01h…1Eh – Buffer delay in 20.83μs units

1Fh – reserved

These bits are R/W. The default value is the delay internal to the codec. The BIOS may add to this value the known delays external to the codec, such as for an external amplifier.</td></tr>
<tr><td>IV</td><td>na</td><td>Information Valid bit

Indicates whether a sensing method is provided by the codec and if information field is valid. This field is updated by the codec.

0h – After codec Reset# de-assertion, it indicates the codec does</td></tr>
</table>

		NOT provides sensing logic and this bit will be Read only. After a sense cycle is completed Indicates that no information is provided on the sensing method 1h – After codec Reset# de-assertion, it indicates the codec provides sensing logic for this I/O and this bit is Read/Write. After clearing this bit by writing "1", when a sense cycle is completed the assertion of this bit indicates that there is valid information in the remaining descriptor bits. Writing "0" to this bit has no effect.
FIP	Codec Default	Function Information Present. This bit set to a '1' indicates that the G[4:0], INV, DL[4:0] (in register 68h), and ST[2:0] (in register 6Ah) bits are supported and are Read/Write capable. This bit set to a '0' indicates that the G[4:0], INV, DL[4:0], and ST[2:0] bits are not supported, and are read-only with a value of zero. This bit is Read Only.

5.9.2.3 Sense Register (Index 6Ah)

Bit	Default	Function
ST[2:0]		Connector/Jack location bits This field describes the location of the jack in the system. 0h – Rear I/O Panel 1h – Front Panel 2h – Motherboard 3h – Dock/External 4h-6h - Reserved 7h – No Connection/unused I/O These bits are Read/Write.
S[4:0]	1h	Sensed bits relates to the I/O being sensed as either output or inputs. Sensed bits (outputs). This field allows for the reporting of the type of output peripheral/device plugged in the jack. Values specified below should be interrogated in conjunction with the SR[5:0] and OR[1:0] bits for accurate reporting. 00h – Data not valid. Indicates that the reported value(s) is invalid. 01h – No connection. Indicates that there are no connected devices. 02h – Fingerprint. Indicates a specific fingerprint value for devices that are not specified or are unknown. 03h – Speakers (8 ohms) 04h – Speakers (4 ohms) 05h – Powered speakers 06h – Stereo headphone 07h – SPDIF Out (electrical) 08h – SPDIF Out (TOS) 09h – Headset (mono speaker left channel and microphone. Read Functions 5 and 4 for matching Microphone) 0Ah – Other. Allows a vendor to report sensing other type of devices/peripherals. SR[5:0] together with OR[1:0] provide information regarding the type of device sensed. 0Bh-0Eh – Reserved 0Fh – Unknown (use fingerprint) 10-1Fh – Reserved Sensed bits (inputs). This field allows for the reporting of the type of input peripheral/device plugged in the jack. Values specified below should be interrogated in conjunction with the SR[5:0] and OR[1:0] bits for accurate reporting. 00h – Data not valid. Indicates that the reported value(s) is invalid. 01h – No connection. Indicates that there are no connected devices. 02h – Fingerprint. Indicates a specific fingerprint value for devices that are not specified. 03h – Microphone (mono) 04h – Stereo Microphone 05h – Stereo Line In (CE device attached) 06h – Mono Line In (CE device attached)

		07h – SPDIF In (electrical) 08h – SPDIF In (TOS) 09h – Headset (mono speaker left channel and microphone. Read Functions 0 to 3 for matching DAC out) 0Ah – Other. Allows a vendor to report sensing other type of devices/peripherals. SR[5:0] together with OR[1:0] provide information regarding the type of device sensed. 0Bh-0Eh – Reserved 0Fh – Unknown (use fingerprint) 10-1Fh – Reserved This field is Read Only.
OR[1:0]	0h	Order Bits These bits indicate the order the sensed result bits SR[5:0] are using. 00 – 10^0 (i.e., Ohms) 01 – 10^1 (i.e., 10 Ohms) 10 – 10^2 (i.e., 100 Ohms) 11 – 10^3 (i.e., 1K Ohms)
SR[5:0]	0h	Sense Result bits These bits are used to report a vendor specific fingerprint or value. (Resistance, impedance, reactance, etc) This field is Read Only.

5.9.3 Slot Mapping Descriptor

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Ch	DAC Slot Mapping	FD3	FD2	FD1	FD0	SD3	SD2	SD1	SD0	CLD3	CLD2	CLD1	CLD0	X	X	X	X	3760h
6Eh	ADC Slot Mapping	LIA3	LIA2	LIA1	LIA0	IMA3	IMA2	IMA1	IMA0	X	X	X	X	X	X	X	MV	3600h

The Slot Mapping Descriptor page provides a way for the controlling software to modify the default slot to DAC/ADC mappings.

Page 01 register 6Ch controls the slots from which the DACs present in the codec will get the data to render.

Bits FD[3:0] control the mapping of the 1st DAC pair (generally the front speakers and headphone), which defaults to slots 3 and 4.

Bits SD[3:0] control the mapping of the 2nd DAC pair (generally the surround speakers), which defaults to slots 7 and 8.

Bits CLD[3:0] control the mapping of the 3rd DAC pair (generally the center and LFE speakers), which defaults to slots 6 and 9.

Page 01 register 6Eh controls the slots onto which the ADCs present in the codec will place data.

Bits LIA[3:0] control the mapping of the Line In ADC, which defaults to slots 3 and 4.

Bits IMA[3:0] control the mapping of the Independent Microphone ADC, which defaults to slot 6.

The MV (Mapping Valid) bit indicates that the values programmed into page offsets 6Ch and 6Eh are valid.

The Slot Mapping registers must default to the values defined as the slot default for the given DAC/ADC, as above.

A CODEC indicates that it does not support a given DAC or ADC by having a read only value of 0000b in the bits associated with the unsupported DAC or ADC.

The MV bit is used to indicate that page 01 offsets 6Ch and 6Eh should be used to steer the slot to DAC/ADC mappings, rather than the DSA[1:0] bits in the Extended Audio ID register 28h. This bit defaults to zero, meaning that the DSA[1:0] bits and the AMAP defaults determine the slot to DAC/ADC mappings. When the software programs values into the DAC Slot Mapping Register or the ADC Slot Mapping Register, it must then set this bit to a "1" to cause the values in these registers to override the DSA[1:0] bits. A read only value of "0" for this bit indicates that the codec does not support this re-mapping capability. All other values should also be "0".

If the codec has the capability to reassign which slots are decoded, then it must implement the above registers as R/W registers. If the codec does not have this capability, the registers must be implemented as read only with value "00h". If any of the codec's slot to DAC mappings are implemented as remappable, all must be remappable. If any of the codec's slots to ADC mappings are implemented as remappable, all must be remappable.

If a codec supports a given DAC or ADC, then the software indicates that the DAC or ADC should decode a different slot or set of slots by programming a different value into the register. Software may indicate that the DAC or ADC is not being used by programming a value of 0h into the associated slot mapping register. This indicates that no slots should be associated with the DAC/ADC. The DAC or ADC should be treated as unused, and the associated output muted. Volume, mute, and other registers associated with the DMA engine should continue to behave normally, but will have no effect.

In the case of a mono DAC/ADC, the second slot in the pair is not used. No data is sent, and the Slot Valid bits are not enabled.

Software is responsible for making sure that the slots specified are compatible with the controller; for instance, some controllers may not be able to accept a stream from a mono ADC on a slot which the controller has implemented as part of a stereo DMA engine.

Valid Values for Slot Mapping Registers	
Value	Slots used by DAC/ADC
3h	Slots 3,4 (Slot 3 for mono)
6h	Slots 6,9 (Slot 6 for mono)
7h	Slots 7,8 (Slot 7 for mono)
Ah	Slots 10,11 (Slot 10 for mono)
0h	None/Not implemented
1,2,4,5,8,9,B,C,D,E,F	Reserved

Table 38. Register Values for Slot Mapping Registers

Note that the S/P-DIF output slot reassignment is controlled by the SPSA[1:0] of the Extended Audio Status and Control Register (Index 2Ah), and is independent of the definition of these registers and the operation of the DAC and ADC slot remapping.

5.10 S/PDIF Concurrency

A S/PDIF capable Codec must support concurrent DA conversion and S/PDIF transmission. But this capability is dependent upon a number of factors

- The format may be PCM, or non-PCM
- The source data may be shared, or independent
- PCM data may already be playing, restricting S/PDIF transmitter AC-link slot or rate options
- S/PDIF data may already be playing, restricting PCM DA conversion AC-link slot or rate options
- The slot assignment may be shared, or independent

- DA conversion rate may match the S/PDIF transmitter rate, or be independent
- SRC implementations differ
- Controller implementations differ

Given the complexity, there needs to be agreement on minimum required concurrency support at 48 kHz, and a simple mechanism that enables the Driver to easily determine whether other S/PDIF configurations are supported (the SPCV bit is described above).

There are two principal sources of audio data to consider:

- "Mixed" data originating from the OS mixer service. This data is typically stereo PCM format and passed on AC-link slots 3&4. Requirement 5.10.1.1 below ensures 48 kHz OS mixer output on AC-link slots 3&4 can be routed to both DAC and S/PDIF transmitter. Option 5.10.2.1 below expands support to 8-48 kHz OS mixer output.
- "Pass-thru" data originating from an "independent S/PDIF source". This data can be PCM, AC-3**, MPEG, DTS, or other format, and is typically passed on AC-link slots 7&8 in 2-ch systems, AC-link slots 6&9 in 4-ch systems, and AC-link slots 10&11 in 6-ch systems. The sample rate of "independent S/PDIF source" data passed across AC-link must match the programmed SPSR (typically 48 kHz). Requirements 5.10.1.21 through 5.10.1.4 ensure availability of independent AC-link slot allocation for "pass-thru" data.

5.10.1 Required concurrency support for S/PDIF transmission (48 kHz operation)

The AC '97 architecture is optimized for 48 kHz operation, at which rate the AC-link signaling protocol reduces to one sample request per frame. Restricting the mixed PCM and independent S/PDIF source data to 48 kHz is a simple way to ensure the greatest number of S/PDIF concurrency options, but requires the OS mixer to perform high quality SRC up-sampling of all PCM data to 48 kHz. Additional SRC capability may be needed if the independent S/PDIF source supports non 48 kHz PCM data.

The following are the minimum concurrency requirements for S/PDIF enabled AC '97 2.3 compliant Codecs.

5.10.1.1 Simultaneous DAC playback and S/PDIF transmission of a single 2-ch 48 kHz PCM stream

All S/PDIF capable Primary Codecs must be configurable to accept 48 kHz PCM data on AC-link slots 3&4 for DA conversion and concurrent S/PDIF transmission. SPCV must indicate valid configuration when programmed as follows:

- Register 2Ch controlling AC-link slots 3&4 DAC sample rates set to "BB80h" (48kHz)
- Register 3Ah, field SPSR[1,0] controlling S/PDIF sample rate set to "10" (48kHz)
- Register 2Ah, field SPSA[1,0] controlling S/PDIF AC-link slot assignment set to "00" (slots 3&4)

This requirement ensures basic support for OS mixer 48 kHz PCM output to DAC and S/PDIF transmitter.

5.10.1.2 Simultaneous DAC playback of a 2-ch 48 kHz PCM stream and S/PDIF transmission of an independent 48 kHz PCM or encoded multichannel stream

2-ch S/PDIF capable Primary Codec must accept 48 kHz PCM data on AC-link slots 3&4 for DA conversion and independent 48 kHz PCM or encoded multichannel data on AC-link slots 7&8 for concurrent S/PDIF transmission. SPCV must indicate valid configuration when programmed as follows:

- Register 2Ch controlling AC-link slots 3&4 DAC sample rates set to "BB80h" (48kHz)
- Register 3Ah, field SPSR[1,0] controlling S/PDIF sample rate set to "10" (48kHz)
- Register 2Ah, field SPSA[1,0] controlling S/PDIF AC-link slot assignment set to "01" (slots 7&8)

4-ch S/PDIF capable Primary Codec must accept 48 kHz PCM data on AC-link slots 3&4 and 7&8 for DA conversion and independent 48 kHz PCM or encoded multichannel data on slot 6&9 for concurrent S/PDIF transmission. SPCV must indicate valid configuration when programmed as follows:

- Registers 2Ch and 2Eh controlling AC-link slots 3&4 and 7&8 DAC sample rates set to "BB80h" (48kHz)
- Register 3Ah, field SPSR[1,0] controlling S/PDIF sample rate set to "10" (48kHz)
- Register 2Ah, field SPSA[1,0] controlling S/PDIF AC-link slot assignment set to "10" (slots 6&9)

These requirements ensure that 2- or 4-ch Codecs w/ S/PDIF can support 2- or 4-ch OS mixer 48 kHz PCM output

while transmitting 48 kHz independent S/PDIF source output, and are compatible with integrated multichannel audio Controllers.

5.10.1.3 Secondary Codec supports simultaneous DAC playback of a 2-ch 48 kHz PCM stream and S/PDIF transmission of an independent 48 kHz PCM or encoded multichannel stream

2-ch S/PDIF capable Secondary Codec must accept 48 kHz PCM data on AC-link slots 7&8 for DA conversion and independent 48 kHz PCM or encoded multichannel data on AC-link slots 6&9 for concurrent S/PDIF transmission. SPCV must indicate valid configuration when programmed as follows:

- Register 2Ch controlling AC-link slots 7&8 DAC sample rates set to "BB80h" (48kHz)
- Register 3Ah, field SPSR[1,0] controlling S/PDIF sample rate set to "10" (48kHz)
- Register 2Ah, field SPSA[1,0] controlling S/PDIF AC-link slot assignment set to "10" (slots 6&9)

This requirement ensures that dual Codec (2-ch + 2-ch w/ SPDIF) configurations can support 4-ch OS mixer 48 kHz PCM output while transmitting 48 kHz independent S/PDIF source output.

5.10.1.4 Primary or Secondary codec supports independent S/PDIF transmission of PCM or encoded stream on slots 10&11

Any Primary or Secondary Codec which supports S/PDIF must accept 48kHz PCM or encoded multichannel data on AC-Link slots 10&11 for concurrent S/PDIF transmission. SPCV must indicate valid configuration when programmed as follows:

- Register 3Ah, field SPSR[1,0] controlling S/PDIF sample rate set to "10" (48kHz)
- Register 2Ah, field SPSA[1,0] controlling S/PDIF AC-link slot assignment set to "11" (slots 10&11)

This requirement ensures that codecs supporting S/PDIF will always be able to support an independent S/PDIF stream transmitted on slots 10&11, without regard to the bit depth, sample rate, or number of channels being transmitted on the PCM stream which may occupy any of slots 3&4, 7&8, and 6&9.

5.10.2 Optional support for rates other than 48 kHz

The following section describes support for two optional features for non 48 kHz AC-link data: upsampling capability and "bit exact" transmission. Support for these options requires unambiguous specification of all sample rates involved:

1. the mixed PCM data rate on slots 3&4 — controlled by the DAC sample rate Register 2Ch
2. the pass-thru data rate on slots 7&8, 6&9, or 10&11 — restricted to rates that match the SPSR setting
3. the S/PDIF transmission rate — controlled by the SPSR field

In the following optional non 48 kHz scenarios the SPCV bit becomes essential to identifying the capability.

5.10.2.1 Simultaneous DAC playback and S/PDIF transmission of a single 2-ch non 48 kHz PCM stream

S/PDIF capable Codec provides SRC capability to accept non 48 kHz PCM data on AC-link slots 3&4 and up-sample to 48 kHz for concurrent DA conversion at 48 kHz and S/PDIF transmission at 48kHz. If supported, SPCV should indicate valid configuration when programmed as follows:

- VRA mode enabled
- Register 2Ch controlling AC-link slots 3&4 DAC sample rates set to "xxxxh" (8-48kHz)
- Register 3Ah, field SPSR[1,0] controlling S/PDIF sample rate set to "10" (48kHz)
- Register 2Ah, field SPSA[1,0] controlling S/PDIF slot assignment set to "00" (slots 3&4)

This option extends the basic support for OS mixer to 8-48 kHz PCM output to DAC and S/PDIF transmitter.

5.10.2.2 Simultaneous DAC playback and S/PDIF transmission of "bit exact" 32, 44.1, or 48 kHz PCM streams

S/PDIF capable Codec provides an output S/PDIF rate which tracks the sample rate for Fs = 32, 44.1 or 48.0 kHz. The S/PDIF transmitter output symbol rate will be 64*Fs as defined by IEC958. In this scenario the S/PDIF transmitter will be running at the same rate as the incoming PCM stream requiring no SRC in the Codec. This allows the Codec to simply pass the PCM data from the source to the destination without sample rate conversion,

thereby preserving 100% of the digital content. If supported, SPCV should indicate valid configuration when programmed as follows:

- Register 2Ch controlling AC-link slots 3&4 DAC sample rates set to "xxxxh" (32, 44.1 or 48kHz)
- Register 3Ah, field SPSR[1,0] controlling S/PDIF sample rate set to "xxh" (32, 44.1, or 48kHz)
- slot 3&4 DAC sample rate matches selected SPSR
- Register 2Ah, field SPSA[1,0] controlling S/PDIF slot assignment set to "00" (slots 3&4)

This option expands "bit exact" S/PDIF transmission to all common S/PDIF rates, not just 48 kHz.

6. Modem AFE Features

6.1 Overview

The purpose of this extension is to define optional interoperable methods for implementing modem analog front-end (AFE) functionality and accessing it via AC-link. This includes:

- Slot assignments for line, handset, and GPIO pin status and control
- GPIO pin status and control definitions
- Modem AFE register definitions
- Power management and wake-up event definitions
- CallerID string transmission via AC-link definitions
- Loopback testing definitions

6.2 Slot Assignments for Modem

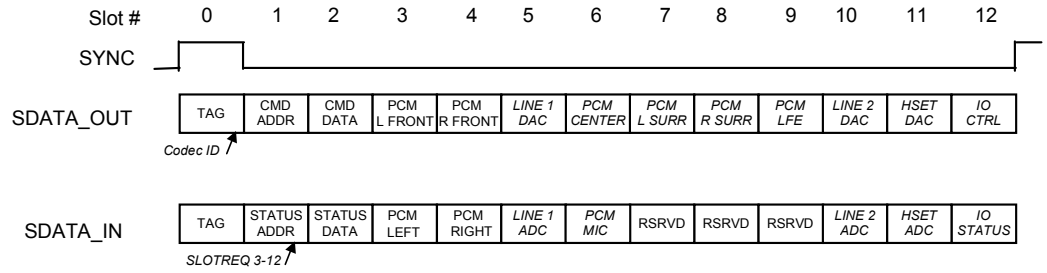


Figure 19. AC-link Slot Assignments

As shown in Figure 19, the line1, line2, and handset streams have been assigned to slots 5, 10, and 11 respectively. As with AC '97 , the leading 16-bits of each slot must contain valid sample data; support for 18 or 20-bits is optional. The following table describes the input and output slot data format.

Input and Output Slots 5, 10, 11: Line1, Line2, Handset ADCs and DACs	
Bit	Description
19-4	16-bit sample (MSB bit 19, LSB bit 4)
3-0	Optional: LSBs of 18 or 20-bit sample

Table 39. Slots 5, 10, and 11-Bit Definitions

Up to 16-bits of GPIO status (input) and control (output) have been directly assigned to bits on slot 12 in order to minimize latency of access. This allows software to monitor changing conditions without the latency imposed by

performing a read operation over the link. Table 40 describes the GPIO output and input slot assignments.

Input and Output Slot 12: GPIO Pin Status and Control	
Bit	Description
19-4	GPIO Pin Status (see Table 41. Recommended Slot 12 GPIO Bit Definitions)
3-1	Vendor specific
0	GPIO_INT mask enabled input pin event interrupt (1=event) (input Slot 12 only)

Table 40. Slot 12-Bit Definitions

6.3 GPIO Pin Definitions

General Purpose Input/Output (GPIO) pins are programmable to have input/output functionality. The data values (status) for these pins are all in one register, with input/output configuration in a separate register. Control of GPIO pins configured for output is achieved by setting the corresponding bit in output slot 12; status of GPIO pins configured for input is returned on input slot 12. The Codec must constantly set the GPIO pins that are configured for output, based upon the value of the corresponding bit position of the control slot 12. The Codec should ignore output slot 12 bits that correspond to GPIO control pins configured as inputs. The Codec must constantly update status on input slot 12, based upon the logic level detected at each GPIO pin configured for input. A GPIO output pin value that is written via slot 12 in the current frame won't affect the GPIO status that is returned in that particular write frame.

This slot 12-based control/status protocol minimizes the latency and complexity, especially for host-based Controllers and host data pump software, and provides high speed monitoring and control, above what could be achieved with command/status slots. For host-based implementations most AC '97 registers can be shadowed by the driver in order to provide immediate response when read by the processor, and GPIO pins configured as inputs should be capable of triggering an interrupt upon a change of status.

The AC-link request for GPIO pin status is always delayed by at least one frame time. Read-Modify-Writes across the AC-link will thus incur latency issues and must be accounted for by the software driver or AC '97 Digital Controller firmware. PCI retries should be kept to a minimum wherever possible.

6.3.1 GPIO Pin Implementation

The modem AFE contains a number of General Purpose Input/Output pins suitable for easy connection with minimal parts to a DAA circuit. There is no requirement that a GPIO, when configured as output, must be able to directly drive a relay coil. The AC '97 Digital Controller is responsible for configuring any GPIOs as outputs on power-up, in order to drive transistors appropriately for DAA control.

When configured as an input, a GPIO must function as a CMOS Schmitt-triggered input for a 3.3V power supply. To conserve power internal pull-ups or pull-downs should not be present. The board designers are responsible for connecting unused pins to DVdd or DVss (or unconnected depending on manufacturer's recommendations).

The GPIOs should be tri-stated to a high impedance state on power-on or a cold reset. It is up to the AC '97 Digital Controller to first enable the output after setting it to the desired state. To prevent overdrive of any transistors, the outputs should have slow rise and fall times. Typical values should be 40 nsec for 10% to 90% of DVdd with a 50 pF load. In addition, the device must sink 2-4 mA at a maximum level of 0.4 V and must source 2-4 mA at a minimum level of 2.4 V.

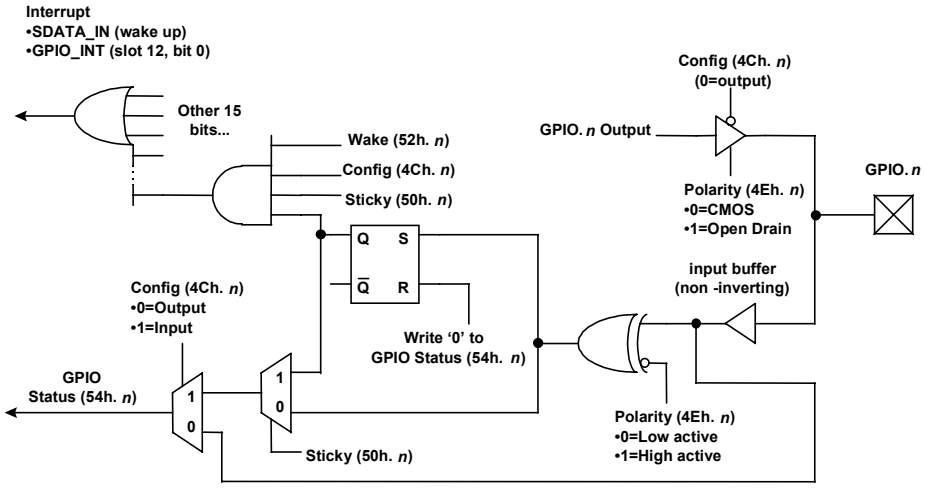


Figure 20. "Conceptual" Example of GPIO Pin Implementation

6.3.2 Recommended Slot 12 GPIO Bit Definitions

Slot 12 (Input and Output): GPIO bits				
Bit	**GPIO**	**Name**	**Sense**	**Description**
19	GPIO15	LINE2_HL2R	out	opt GPIO / HANDSET_TO_LINE2 relay control (out)
18	GPIO14	LINE2_PULSE	In/out	opt GPIO / Line 2 pulse dial (out)
17	GPIO13	LINE2_LCS	in	Loop Current Sense Line 2
16	GPIO12	LINE2_CID	out	Caller ID path enable Line 2
15	GPIO11	LINE2_RI	in	Ring Detect Line 2
14	GPIO10	LINE2_OH	out	Off Hook Line 2
13	GPIO9	LINE12_RS	in/out	opt GPIO / International Bit 3 / Line 1/2 RS (out)
12	GPIO8	LINE12_DC	in/out	opt GPIO / International Bit 2 / Line 1/2 DC (out)
11	GPIO7	LINE12_AC	in/out	opt GPIO / International Bit 1 / Line 1/2 AC (out)
10	GPIO6	LINE1_HOHD	in/out	opt GPIO / HANDSET off hook detect (in)
9	GPIO5	LINE1_HL1R	in/out	opt GPIO / HANDSET to Line 1 relay control (out)
8	GPIO4	LINE1_PULSE	in/out	opt GPIO / Line 1 pulse dial (out)
7	GPIO3	LINE1_LCS	in	Loop Current Sense Line 1
6	GPIO2	LINE1_CID	out	Caller ID path enable Line 1
5	GPIO1	LINE1_RI	in	Ring Detect Line 1
4	GPIO0	LINE1_OH	out	Off Hook Line 1
1-3		Vendor specific		vendor optional
0		GPIO_INT		GPIO_INT (uses same logic as wake-up event)

Table 41. Recommended Slot 12 GPIO Bit Definitions

AC '97 makes no requirement on the number of GPIOs or their use, only that they be implemented as general

purpose. Recommended bit definitions are provided for maximum interoperability, and should be followed wherever possible.

The suggested use for the International Bits 1-3 is to implement LINE12_AC, LINE12_DC, and LINE12_RS, which, when set to one, adjust the DAA AC impedance, DC impedance, and Ring Detect sensitivity to alternate values more suitable for some non-North American countries. These outputs have effect on both Line 1 and Line 2 (it is assumed that both DAAs reside in the same country).

Outputs LINE1_PULSE and LINE2_PULSE control pulse dial relays, separate from the Off Hook relays, used in DAAs for some non-North American DAAs.

GPIO_INT has been added to build upon the logic that has already been implemented within the Codec to detect a change in GPIO input state and trigger a wake-up event. When the Codec is NOT in power-down mode any input GPIO change can be enabled by the wake-up mask to generate GPIO_INT=1, to indicate to the controller or driver that the GPIO state has changed and should be updated in memory. The controller acknowledges and clears a wake-up event or GPIO_INT by writing a 0 to the corresponding bit in Register 54h. This supports shadowing of Codec registers in memory by potentially eliminating polling.

6.4 Modem Codec Cost Reduction Options

6.4.1 Elimination of the On-board Modem Speaker

Modem subsystems currently rely on an on-board speaker for call progress monitoring. Routing call signals through the system speakers enables cost reduction via elimination of the redundant speaker. There is a hardware-dependent analog solution and a hardware-independent digital solution (which supports analog or USB speakers).

- Analog solution: The system designer can route an analog mix of the modem Tx and Rx signals through PHONE input of the AC '97 analog mixer. This requires that the modem control task have access to AC '97 audio driver interface PHONE volume and mute controls, and introduces a dependency on the user's preferred master audio volume and mute settings[12] (which the modem driver should not attempt to access).
- Digital solution: The modem driver designer can route digital copies of the modem Rx (ADC) and Tx (DAC) streams (or perhaps just the digitized pre-echo-canceled modem Rx stream from the ADC) into the system-wide software audio mixer. As with the analog solution, this introduces a dependency on the user's preferred master audio volume and mute settings. For this technique to be cost-effective a soft modem implementation is probably required.

For soft modem implementations AC '97 2.2 recommends the digital call progress monitoring solution[13].

6.4.2 Internal PHONE and MONO_OUT Connections (AMC '97)

The AC '97 PHONE input was designed to support monitoring of analog telephony signals, such as speakerphone or call progress, through the audio subsystem and speakers. The AC '97 MONO_OUT was designed to support routing of analog system audio signals (PHONE and PC_BEEP excluded) to the modem subsystem.

Prior to controller-less modems and low latency digital audio, support for voice required:

1. controller functionality to encode and decode digital voice data
2. a dedicated voice Codec
3. analog connections between the modem and audio subsystems

[12] Depending on the OS driver model, access to the analog mixer topology may be supported via standard interface calls. These calls allow access to mixer mute/volume controls and eliminate the need for a proprietary audio driver interface. Refer to the appropriate OS Audio Device Class Reference Specifications.

[13] The digital solution isolates the final call progress rendering hardware. The analog solutions do not lend themselves easily to audio upgrades or the use of USB speaker solutions. Refer to the appropriate OS Audio Device Class Reference Specifications

Current voice modem implementations migrate the controller functionality into the modem driver, eliminate the redundant voice Codec, and rely on low latency digital streaming between the modem and audio drivers.

AMC designs may optionally implement the PHONE and MONO_OUT connections internally to save package pins. For certification reasons, care should be taken to limit the bandwidth of analog audio signals coupled to the modem Tx via MONO_OUT.

6.5 Wake-up and Power Management Event (PME#) Support

Ring and handset offhook detect are examples of events that might need to wake-up a PC that has suspended into a low power state. Wake-up on an audio event could eventually become practical.

Revision 1.x AC '97 architecture enables fine granular power management of the AC-link and the individual subsections within the Codec. However it does not support system wake requests triggered by external events. Power management, or wake, event support for a modem is a key feature of the Intel® Instantly Available PC power management architecture and must be fully comprehended by the Extended AC '97 architecture. Support for wake-up must be comprehended for various configurations of AC '97 and (A)MC '97 , whether for single Codec, or split partitioned Primary/Secondary Codec implementations.

The Instantly Available PC power management architecture specifies a Vaux supply that is designed to support specific "always active" functions while the majority of the PC is powered down. 5.0 V *and* 3.3 V Vaux supplies are available on the motherboard, and a 3.3 V Vaux supply pin is currently being added to the PCI slot definition. The integrity(?) of the Vaux supply will depend on the power supply source.

6.5.1 Combined Audio/Modem AFE Codec (AMC '97)

For AMC '97 combined Audio/Modem AFE implementations the Codec, AC-link and portions of the AC '97 Digital Controller which provide wake-up functionality, all must be powered by Vaux as illustrated in Figure 21:

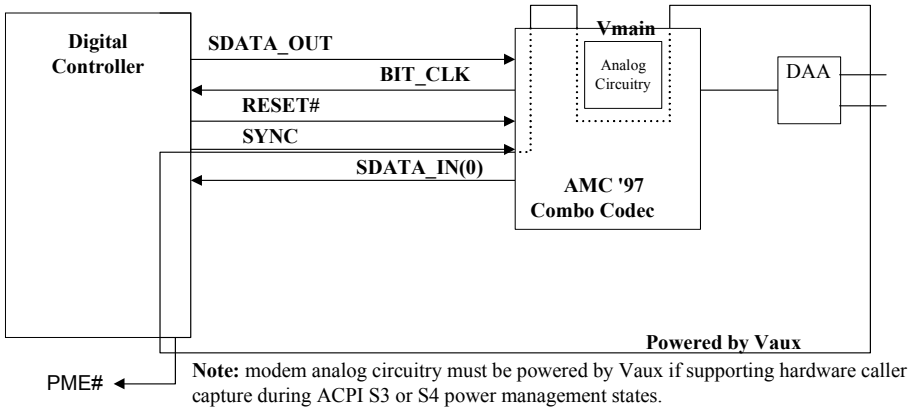


Figure 21. Combined Audio / Modem AFE Auxiliary Power Distribution

The Codec and AC-link are programmed to a low power state (see Figure 22) and, upon detection of a power management event, are brought back to the active state by executing a warm reset sequence as shown in Figure 23.

Figure 22 shows the AC '97 Digital Controller placing the AC-link into its lowest power state by programming the Codec's Power-down Control/Status Register with bit(12) = 1 (PR4) .

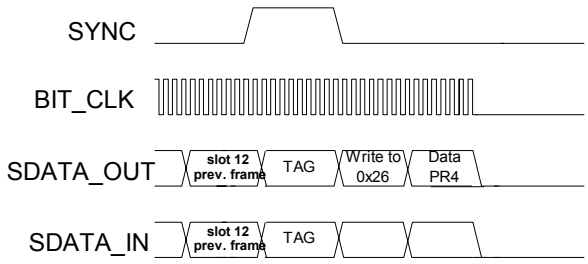


Figure 22. AC-link Low Power Mode

In response to this command BIT_CLK and SDATA_IN Codec, and SDATA_OUT controller outputs go low and stay low.

AC-link when programmed to its low power mode, can be reactivated only by the device driver, which can write to an AC '97 Digital Controller register causing it to signal a cold or warm reset on the AC-link. A warm reset, which will not alter the current AC '97 registers, is signaled by driving SYNC high for a minimum of 1µs in the absence of BIT_CLK.

Within normal audio frames SYNC is a synchronous Codec input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used to signal a warm reset to the AC '97 Codec.

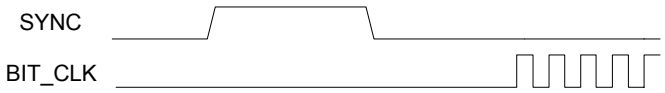


Figure 23. AC-link Warm Reset

In an AMC '97 implementation, where the audio/modem AFE Codec and AC-link are both completely powered by Vaux, an enabled power management event detected at the modem interface causes the assertion of the PME# signal to the system. PME# assertion causes the system to resume so that the modem event can be serviced. The device driver must first reestablish communications with the Codec to command the AC '97 Digital Controller to execute a warm reset to the AC-link. Figure 24 illustrates the entire sequence:

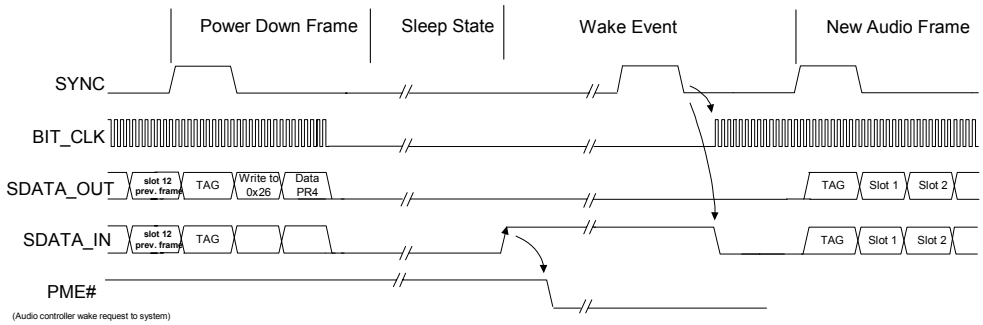


Figure 24. AC-link Power-down/Up Sequence

The rising edge of SDATA_IN causes the AC '97 Digital Controller to assert its PME# to the system's ACPI controller. The AMC '97 Codec must keep SDATA_IN high until it has sampled SYNC first having gone high, and

then low. PME# is cleared out in the AC ‘97 Digital Controller by system software, asynchronous to AC-link activity. The AC ‘97 Digital Controller must always monitor the Codec’s ready bit before sending data to it.

6.5.2 Split Partitioned Implementations (AC ‘97 + MC ‘97)

In a split partitioned implementation, where separate audio and modem AFE Codecs are employed, the MC ‘97 Codec, its DAA, a common clock oscillator, and portions of the AC ‘97 Digital Controller are powered by Vaux. The AC ‘97 audio-only Codec is powered via its normal DVdd, and AVdd supplies, and as such is shut completely off when the system enters a sleeping state. Figure 25 shows an example of a split partitioned Codec implementation.

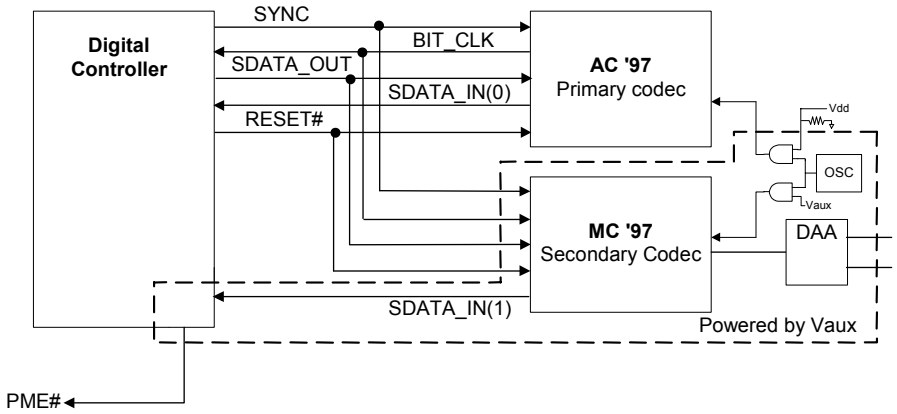


Figure 25. Split Partitioned Design Example

Once the system enters a sleeping state Vdd shuts off, which causes the oscillator input to the AC ‘97 to go low and remain low. Clocking remains active at the MC ‘97, which continues to look for ring detection and Caller ID data while the rest of the system sleeps. A wake or power management event causes the MC ‘97 to transition its SDATA_IN from low to high, which in turns causes the AC ‘97 Digital Controller to assert PME# to the system. Once the main power has been reapplied the device driver executes a cold or warm AC-link reset followed by the restoration of any saved off- functional context. Following SDATA_IN’s low-to-high transition as a result of a Power Management event, it must remain high until either a warm or cold reset is observed on the AC-Link.

6.5.3 Wake-up and Voltage Sequencing

AC ‘97 Codecs have both analog and digital supply pins defined. There are no voltage sequencing requirements for AVdd and DVdd specifying which voltage source ramps up or down first.

In an “Always Ready, Power Management”-capable PC the main Vdd voltage rails will be shut off under program control in order to achieve a very low power state, yet remain connected. Auxiliary power (Vaux), will remain active in the system to keep portions of the modem “alive”[14]. Codec designs that support separate voltage inputs for analog and digital sections must comprehend this so that no device damage or malfunction can occur as a result of the main voltage dropping off while the auxiliary supply remains active.

6.5.4 Wake-up and Caller ID Decode in the Controller and/or Codec

The resume time for a PC in D3 low power state makes it unlikely that a driver will completely load in time to wake-up the AC ‘97 Digital Controller and enable it to capture Caller ID data on the line. Therefore either the AC ‘97 Digital Controller or (A)MC ‘97 Codec must be able to store this information while the driver continues to

[14] This includes all logic required to detect the external wake event, and then to report it across the AC-link.

initialize. In the case of the combined Codec (AMC '97), the entire Codec, AC-link, and portions of the AC '97 Digital Controller are powered by Vaux which enables Caller ID decode and store to be done either by the controller or by the modem AFE Codec. However in the case of the split partitioned design, only the MC '97 SDATA_IN signal on the AC-link is powered while the remainder of the AC-link is un-powered. In this case the Caller ID decode and store operations must be supported in the MC '97 Codec.

If the maximum delay from a PME# event to power pins on the PCI Bus at 95% full value is under 2 seconds, controller manufacturers may be able to load the Caller ID code and wait for the incoming data before the driver has an opportunity to configure the part and assign it resources. The controller then may present the Caller ID data to the driver when it is loaded.

The resume time for a PC in D3 cold also precludes host-based processing of the caller ID burst, in both the U.S. and Europe. (A)MC '97 Codecs which serve as the AFE for host-based modem implementations may find it attractive to support Caller ID decode functionality in addition to simple wake-up on ring detect. Such a Codec would be able to automatically decode and save the caller ID string until the PC system and AC '97 Digital Controller have resumed.

The optional CID1 and CID2 bits in the Miscellaneous Modem AFE Status and Control Register have been defined to indicate to the awakened AC '97 Digital Controller that decoded caller ID string data is available for Line1 (CID1=1) or Line2 (CID2=1). ADC input slots 5 (for Line 1) and 10 (for Line 2) can be used to transfer the caller ID string data, two bytes per AC-link input frame until completed, at which time the CIDn bit automatically resets (goes inactive).

The AC '97 Digital Controller initiates the stored caller ID string transfer by strobing (writing) CIDn=1 and subsequently reading data from input slot 5 (for Line 1) or 10 (for Line 2) until the tag bit and (and as a consequence, CIDn) becomes inactive. To prevent unnecessary register access to Register 3Ch, the tag bit should go inactive for at least one AC-link frame between Caller ID string transfer and ADC transfer. A strobe (write) of CIDn=0 will clear or cancel the caller ID transmission and reset the CIDn indicator. Once the CIDn bit is reset (automatically or manually), the slot resumes transfer of ADC input data.

Data from the caller ID string can be handled two ways. It can either be demodulated only (raw) or demodulated and preprocessed to delete the channel seizure time and mark signal time, etc. It requires slightly more RAM (approx. 50 bytes) to retain a raw string, but less decoder intelligence. The CIDR bit in the Miscellaneous Modem AFE Status and Control Register indicates which method the Codec caller ID supports. CIDR=1 indicates that stored caller ID data is raw.

6.6 Modem AFE Register Definitions

6.6.1 Extended Modem ID Register (Index 3Ch)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Ch	Extended Modem ID	ID1	ID0	x	x	x	x	x	x	x	x	x	CID2	CID1	HSET	LIN2	LIN1	xxxxh

The extended modem ID is a read/write register that primarily identifies the enhanced Codec's modem AFE capabilities. The default value will depend on features and hardware configuration. Writing any value to this register performs a warm modem AFE reset (register range 3C-56h), including GPIO (register range 4C-54h). The warm reset causes all affected registers to revert to their default values. Note: for AMC '97 parts the audio and modem AFE should be logically independent (writes to Register 00h resets audio only).

- LIN1=1 indicates 1st line is supported
- LIN2=1 indicates 2nd line is supported
- HSET=1 indicates handset DAC/ADC is supported
- CID1=1 indicates that caller ID decode for line 1 is supported
- CID2=1 indicates that caller ID decode for line 2 is supported
- ID1, ID0 is a 2-bit field which indicates the Codec configuration: Primary is 00; Secondary is 01, 10, or 11

If LIN1=1, then the Codec is an (A)MC '97 , and all modem functionality should be implemented and controlled via

the newly-defined Extended AC '97 registers. In particular, it is required that the following functionality NOT be implemented as defined in the original AC 97 Component Specification:

- Reset Register (Index 00h) bit 1: Modem line Codec support (ID1)
- Reset Register (Index 00h) bit 6-9 audio DAC and ADC resolution do not have any MAFE resolution information
- General Purpose Register (Index 20h) bits 10, 11: Local Loopback (LLBK) and Remote Loopback (RLBK)
- Modem Rate (Index 24h) Register
- Power-down/Ctrl/Stat (Index 26h) bits 4 ,15: Modem Ready (MDM) and Modem DAC/ADC off (PR7)

Modem DAC and ADC resolution is by default 16-bits. Modem interoperability is not expected between AC `97 Controller/Codec pairs that aren't designed to work together, but vendor specific methods can be used to identify and support 18- or 20-bit resolution. For example, an AC `97 Controller could determine the modem DAC/ADC resolution in an MC or AMC Codec by inspecting the Vendor ID Registers.

The value after cold or register reset for this register is constant, and depends on features supported and hardware configuration as Primary or Secondary Codec.

6.6.2 Extended Modem Status and Control Register (Index 3Eh)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Eh	Ext'd Modem Stat/Ctrl	PRH	PRG	PRF	PRE	PRD	PRC	PRB	PRA	HDAC	HADC	DAC2	ADC2	DAC1	ADC1	MREF	GPIO	FFxxh

The Extended Modem Status and Control Register functions similarly to the original AC '97 Power-down Control/Status Register, located at index 26h. The (A)MC '97 Codec must restrict modem and handset power-down control/status to this register since all of the functions are provided here. Therefore, the (A)MC '97 Codec (and AC '97 Digital Controller, of course) must not implement MDM and PR7 in Register 26h and use what is included here. When the GPIO section is powered down, all outputs must be tri-stated and input slot 12 should be marked invalid when the AC-link is active. When slot 12 is invalid, Register 54h (GPIO Pin Status Register) will report 0s. In addition the Codec should force SDATA_IN slot 12 to all 0s.

Bits 7-0 are read only, 1 indicates modem AFE subsystem readiness:

- GPIO=1 indicates GPIO ready
- MREF=1 indicates Modem Vref's up to nominal level
- ADC1=1 indicates Modem Line 1 ADC ready
- DAC1=1 indicates Modem Line 1 DAC ready
- ADC2=1 indicates Modem Line 2 ADC ready
- DAC2=1 indicates Modem Line 2 DAC ready
- HADC=1 indicates Handset ADC ready
- HDAC=1 indicates Handset DAC ready

Bits 15-8 are read/write and control modem AFE subsystem power-down. For AMC '97 implementations that use a common AREF and MREF, both power-down bits must be low for disabling the reference.

- PRA=1 controls GPIO power-down
- PRB=1 controls Modem Vref off
- PRC=1 controls Modem Line 1 ADC off
- PRD=1 controls Modem Line 1 DAC off
- PRE=1 controls Modem Line 2 ADC off
- PRF =1 controls Modem Line 2 DAC off
- PRG=1 controls Handset ADC off
- PRH=1 controls Handset DAC off

The default value after cold or register reset for this register (FFxxh) is all extended features are powered down (D15-D8=1). The feature readiness status should always be accurate (D7-D0=x).

6.6.3 Modem Sample Rate Control Registers (Index 40h – 44h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	Line1 DAC/ADC Rate (input, output slot 5)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
42h	Line2 DAC/ADC Rate (input, output slot 10)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
44h	Handset DAC/ADC Rate (input, output slot 11)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

For modem AFE, each DAC/ADC pair is governed by a read/write modem sample rate control register that contains a 16-bit unsigned value between 0 and 65535, representing the rate of operation in Hz. Any number written over BB80h will cause the sample rate to be 48 kHz. For all rates, if the value written to the register is supported, that value will be echoed back when read; otherwise the closest (higher in case of a tie) rate supported is returned.

Table 42 defines the recommended set of sample rates for consideration. Although bit fields could be used to support the relatively few recommended sample rates, a full 16-bit register was chosen as the most flexible way to support future expandability.

Support for the non-integer sample rates, 13,714.28 (96000/7), 8228.57 (57600/7), and 10285.71 (72000/7), requires that the Codec automatically recognize the non-integer rate from the integer portion.

Recommended (+) sample rates for modem AFE (Hz)			
Sample rate	**D15-D0**	**line1, line2**	**handset**
7200	1C20	+	
8000	1F40	+	+
8228.57 (57600/7)	2024	+	
8400	20D0	+	
9000	2328	+	
9600	2580	+	
10285.71 (72000/7)	282D	+	
12000	2EE0	+	
13,714.28 (96000/7)	3592	+	
16000	3E80	+	+
19200	4B00	+	

Table 42. Sample Rates for Modem AFE (Hz)

Note: To comply with ITU-T modem recommendations, sample rates must be generated to a tolerance of +/- 0.01%. This includes crystal tolerance, including variations over voltage, temperature, and age.

The default value after cold or register reset for these registers (BB80h) is 48 kHz.

6.6.4 Modem DAC/ADC Level Control Registers (Index 46h – 4Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
46h	Line 1 DAC/ADC Level	Mute	x	x	x	DAC3	DAC2	DAC1	DAC0	Mute	x	x	x	ADC3	ADC2	ADC1	ADC0	8080h
48h	Line 2 DAC/ADC Level	Mute	x	x	x	DAC3	DAC2	DAC1	DAC0	Mute	x	x	x	ADC3	ADC2	ADC1	ADC0	8080h
4Ah	Handset DAC/ADC Level	Mute	x	x	x	DAC3	DAC2	DAC1	DAC0	Mute	x	x	x	ADC3	ADC2	ADC1	ADC0	8080h

These read/write registers control the modem AFE DAC and ADC levels. DAC levels are defined to be the same as AC '97 Play Master Volume Register (2-6h minus 5th and 6th bits); ADC levels are defined to be the same as AC '97 Record Gain Registers (1C-1Eh).

The default value after cold or register reset for these registers (8080h) corresponds to 0 dB DAC attenuation with mute on, 0 dB ADC gain/attenuation with mute on.

6.6.5 GPIO Pin Configuration Register (Index 4Ch)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
4Ch	GPIO Pin Config (0 =output, 1=input)	GC15	GC14	GC13	GC12	GC11	GC10	GC9	GC8	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	FFFFh

The GPIO Pin Configuration is a read/write register that specifies whether a GPIO pin is configured for input (1) or for output (0), and is accessed via the standard slot 1 and 2 command address/data protocols.

If a GPIO pin is implemented, the respective GCx bit should be read/writable and set to 1. If a GPIO is not implemented, then the respective GCx bit should be read-only and set to 0. This informs the software how many GPIO pins have been implemented. It is up to the AC '97 Digital Controller to send the desired GPIO pin value over output slot 12 in the outgoing stream of the AC-link before configuring any of these bits for output.

The default value after cold or register reset for this register (FFFFh), is all pins configured as inputs.

6.6.6 GPIO Pin Polarity/Type Register (Index 4Eh)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
4Eh	GPIO Pin Polarity/Type (0 =low, 1=high active)	GP15	GP14	GP13	GP12	GP11	GP10	GP9	GP8	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	FFFFh

The GPIO Pin Polarity/Type is a read/write register that defines GPIO Input Polarity (0=Low, 1=High active) when a GPIO pin is configured as an Input. It defines GPIO Output Type (0=CMOS, 1=OPEN-DRAIN) when a GPIO pin is configured as an Output.

The default value after cold or register reset for this register (FFFFh) is all pins active high. Non-implemented GPIO pins always return 1s.

6.6.7 GPIO Pin Sticky Register (Index 50h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
50h	GPIO Pin Sticky (0 =not sticky, 1=sticky)	GS15	GS14	GS13	GS12	GS11	GS10	GS9	GS8	GS7	GS6	GS5	GS4	GS3	GS2	GS1	GS0	0000h

The GPIO Pin Sticky is a read/write register that defines GPIO Input Type (0=Non-Sticky, 1=Sticky) when a GPIO pin is configured as an input. GPIO inputs configured as Sticky are cleared by writing a 0 to the corresponding bit of the GPIO Pin Status Register 54h (see below), and by reset.

The default value after cold or register reset for this register (0000h) is all pins non-Sticky. Unimplemented GPIO pins always return 0s. Sticky is defined as Edge sensitive, Non-Sticky as Level-sensitive.

6.6.8 GPIO Pin Wake-up Mask Register (Index 52h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
52h	GPIO Pin Wake-up (0 =no int, 1=yes int)	GW15	GW14	GW13	GW12	GW11	GW10	GW9	GW8	GW7	GW6	GW5	GW4	GW3	GW2	GW1	GW0	0000h

The GPIO Pin Wake-up is a read/write register that provides a mask for determining if an input GPIO change will generate a wake-up or GPIO_INT (0=No, 1=Yes). When the AC-Link is powered down (Register 26h PR4 = 1 for Primary Codecs), a wake-up event will trigger the assertion of SDATA_IN (the AC-Link wake-up protocol is defined in Section 3.5.2). When AC-link is powered up, a wake-up event will appear as GPIO_INT=1 on bit 0 of input slot 12.

An AC-Link wake-up Interrupt is defined as a 0 to 1 transition on SDATA_IN when the AC-Link is powered down (Register 26h PR4=1). GPIO bits that have been programmed as Inputs, Sticky and Pin Wake-up, upon transition either (high-to-low) or (low-to-high) depending on pin polarity, will cause an AC-Link wake-up event (transition of SDATA_IN from 0 to 1), if and only if the AC-Link was powered down.

The default value after cold or register reset for this register (0000h) defaults to all 0s specifying no wake-up event. Non-implemented GPIO pins always returns 0s.

6.6.9 GPIO Pin Status Register (Index 54h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
54h	GPIO Pin Status (slot 12, bits 15-0)	GI15	GI14	GI13	GI12	GI11	GI10	GI9	GI8	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0	xxxxh

The GPIO Status is a read/write register that reflects the state of all GPIO pins (inputs and outputs) on slot 12. The value of all GPIO pin inputs and outputs comes in from the Codec every frame on slot 12, but is also available for reading as GPIO Pin Status via the standard slot 1 and 2 command address/data protocols. GPIO inputs configured as Sticky are cleared by writing a 0 to the corresponding bit of this Register 54h.

Bits corresponding to unimplemented GPIO pins should be forced to zero in this register and input slot 12.

GPIO bits that have been programmed as Inputs and Sticky, upon transition either (high-to-low) or (low-to-high) depending on Pin polarity, will cause the individual GI bit to go asserted 1, and remain asserted until a 0 is written to that bit. The only way to set the desired value of a GPIO output pin is to set the control bit in output slot 12.

The default value, if configured as an input, after cold or register reset for this register is always the state of the GPIO pin.

6.6.10 Miscellaneous Modem AFE Status and Control Register (Index 56h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
56h	Miscellaneous Modem AFE Stat/Ctrl	CID2	CID1	CIDR	MLNK	x	HSB2	HSB1	HSB0	x	L2B2	L2B1	L2B0	x	L1B2	L1B1	L1B0	x000h

This read/write register defines the Loopback modes available for the modem line and handset ADCs/DACs described in section 7.7. It also supports the optional CID bits described in Section 6.5.4.

- L1B2-0 controls Line 1 loopback modes (or disabled)
- L2B2-0 controls Line 2 loopback modes (or disabled)
- HSB2-0 controls Handset loopback modes (or disabled)
- MLNK controls a Secondary Modem Codec's AC-link status (see below)
- CID1=1 indicates caller ID decode for Line 1 is supported
- CID2=1 indicates caller ID decode for Line 2 is supported
- CIDR=1 indicates that caller ID data is "raw" (demodulated but not decoded; includes seizure, marks, etc.)

AC '97 2.0 defined the modem MLNK bit as a flag which, when set, indicates to the modem Codec that the AC-link

is about to be placed in a low power mode with BIT_CLK stopped. In a typical AC + MC, or AMC configuration the audio Codec is deployed as the Primary Codec, and the modem Codec is deployed as the Secondary Codec. Setting the MLNK bit, given one of these common configurations is problematic. The issue is that there is no standard mechanism for the modem driver to know when the audio driver is about to program the audio Codec to PR4, and so when it should set the MLNK bit. The audio and modem drivers must remain mutually exclusive of each other. Therefore the MLNK bit, in any audio/modem configuration with the modem Codec deployed as the Secondary Codec is meaningless as specified in AC '97 2.0.

New MLNK bit Definition: MLNK indicates to the modem Codec that its modem driver is preparing the modem subsystem to enter the $D3_{hot}$ state.

The modem Codec's behavior following the setting of its MLNK bit is dependent upon whether the Codec has been configured as the Primary or Secondary AC-link Codec; for details refer to Section 7.3.

The default value after cold or register reset for this register (x000h) is all loopbacks disabled. The default value for the CID1, CID2, and CIDR bits depend on the caller ID features.

6.7 Loopback Modes for testing

In Local Analog Loopback mode, the analog output from DAC is connected to the analog input of the associated ADC. The DAC output pin(s) are muted and the ADC input pin(s) are ignored. In Remote Analog Loopback mode, The ADC input pin(s) are connected to the DAC pin(s) in addition to the ADC input. The DAC output is ignored.

Bit	Name	Function
2-0	L1B2-L1B0	Modem Line 1 Loopback enable 000 = Disabled (default) 001 = ADC Loopback 010 = Local Analog Loopback 011 = DAC Loopback 100 = Remote Analog Loopback 101 -111 = Vendor optional
6-4	L2B2-L2B0	Modem Line 2 Loopback enable 000 = Disabled (default) 001 = ADC Loopback 010 = Local Analog Loopback 011 = DAC Loopback 100 = Remote Analog Loopback 101-111 = Vendor optional
10-8	HSB2-HSB0	Handset Loopback enable 000 = Disabled (default) 001 = ADC Loopback 010 = Local Analog Loopback 011 = DAC Loopback 100 = Remote Analog Loopback 101-111 = Vendor optional

Table 43. Modem Loopback Control Bit Definitions

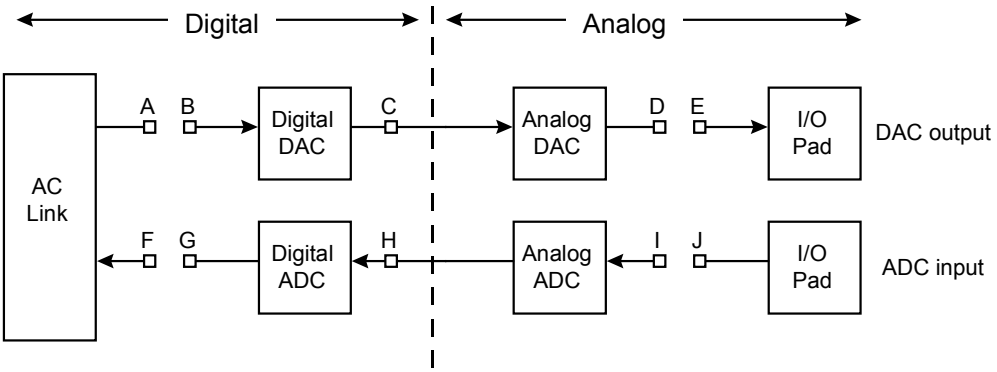


Figure 26. Loopback points

6.7.1 ADC Loopback '001'

The ADC Loopback takes the line input signal to the ADC and routes it back to the Line output. This loop includes the analog functions in the receive and transmit path. The path is from the ADC input all the way to point G where it is then looped back to point B and out to the DAC output.

6.7.2 Local analog Loopback '010'

The appropriate outgoing slot of the AC-link is passed through the DAC and the analog filters, looped back through the ADC, then onto the appropriate incoming stream slot of the AC-link. This is commonly used in modem modes to troubleshoot problems. This path is from the link (point A) to point D where it is looped back to point I and back through the ADC to the link.

6.7.3 DAC Loopback '011'

This digital test loops back the digital transmit path (outgoing stream) to the digital receive path (incoming stream). This path is from the link (point A) to through the Digital portion of the DAC to point C where it is looped back to point H and back through the digital section of the ADC.

6.7.4 Remote analog Loopback '100'

The Line input signal is routed back to the Line output. This loop includes the analog receive functions, but no ADC or DAC. This path is from the ADC input to point J where it is looped back to point E and out to the DAC output.

7. Power Management

AC ‘97 Codecs can operate at reduced power when no activity is required, and need to be a fully static design, so that when the clock is stopped the registers will not lose their values. For 2-channel audio Codecs low power states are controlled by bits D8-D15 in the Powerdown Register, 26h (see Table 29 for full definitions). Monolithic multichannel Codecs additionally use bits D11-D13 in the Extended Audio Status and Control Register, 2Ah, to manage their additional DACs. For example, when setting L&R DACs off (PR1) a multichannel audio driver should also check the Surround, Center and LFE DACs.

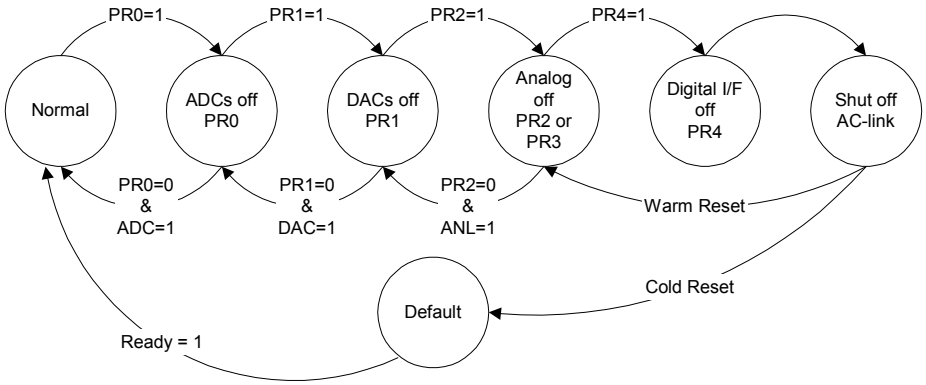


Figure 27. One example of AC ‘97 Powerdown/Powerup flow

Figure 27 illustrates one example procedure to do a complete powerdown of AC ‘97. From normal operation, sequential writes to the Powerdown Register are performed to powerdown AC ‘97 a subsection at a time. After all subsections have been shut off, a final write (of PR4) can be executed to shut down the AC ‘97’s digital interface (AC-link). The part will remain in sleep mode with all its registers holding their static values. To wake-up, the AC ‘97 Controller will send a pulse on the sync line issuing a warm reset. This will restart AC ‘97’s digital interface (resetting PR4 to zero). AC ‘97 can also be awakened with a cold reset. A cold reset will cause a loss of values of the registers since this will set them to their default states. When a section is powered back on again, the Powerdown Control/Status Register (index 26h) should be read to verify that the section is ready (i.e. stable) before attempting to use it in any operation.

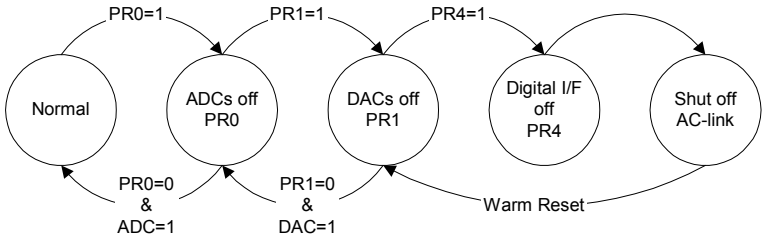


Figure 28. AC ‘97 Powerdown/Powerup flow with analog mixer still alive

Figure 28 illustrates a state when all the analog mixer paths should work with the static volume settings that are contained in their associated registers. This is used when the user could be playing a CD (or external LINE_IN source) through AC ‘97 to the speakers but has most of the system in low power mode. The procedure for this

follows the previous one, except that the analog mixer is not shut down.

7.1 Power Management "D State" Mappings for Audio Codecs

The ACPI and PCI Bus Power Management Interface specifications define an accepted set of device power management states (D0 – D3). An audio device driver written to comprehend these power management specifications must map each supported system-side D state to an audio Codec-specific power savings mode using the PR bits.

A high-level set of expectations for the mapping of D States to audio feature availability, power consumption, resume latency, etc., is available in the Microsoft Audio Device Class Power Management Reference Specification** located at:

http://www.microsoft.com/hwdev/download/audpmspc.rtf

Table 44 details a lower-level mapping of the audio subsystem D states to the recommended AC '97 Codec power savings PR settings.

PR<0:6> + EAPD									+12 Vmain	+5Vaa from +12 Vmain	+3.3 Vmain	+3.3 Vaux	Comments
	EAPD	HP Amp	Int. CLK	AC-Link	Mixer Vref	Mixer	DAC	ADC					
Device State	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**					
D0	0	0	0	0	0	0	0	0	On	On	On	On	All on
D1	0	0	0	0	0	0	***1***	***1***	On	On	On	On	-DAC, -ADC
D2	***1***	***1***	0	0	0	***1***	1	1	On	On	On	On	-Mix, -Amp
$D3_{hot}$	1	1	***1*** Note 3	0 Note 1	1/0 Note 2	1	1	1	On	On	On	On	-int clk -hp amp
$D3_{cold}$	-	-	-	-	-	-	-	-	Off	Off	Off	On	unpowered

Table 44. Recommended Audio Codec D state to PR bit mapping

Note 1: PR4 (AC-link BIT_CLK stopped), is not recommended for $D3_{hot}$. Under certain circumstances disabling of the AC-link BIT_CLK during $D3_{hot}$ may interfere with Secondary modem Codec operation, and so is not recommended. For details on this clocking issue refer to Section 8.6 (AC + MC clocking considerations).

Note 2: Disabling of Vref (i.e., PR3 = 1) will impose a hardware-dependent power-up delay upon resuming. An audio vendor must weigh the incremental power savings provided by setting PR3, with the added resume latency it imposes when deciding how the audio driver is to treat this bit while preparing to enter $D3_{hot}$.

Note 3: PR5 enables a Primary AC Codec to enter lowest power state while still providing BIT_CLK to Secondary Codecs on the AC-link. Depending on how PR5 is implemented, AMC or AC + MC designs may need to manage PR5 identically to PR4.

When the system transitions to a deep sleep state of S3, S4 or S5, all main voltage rails are shut off leaving the audio Codec unpowered. During each transition to $D3_{hot}$, the audio driver must assume that it will ultimately end up in $D3_{cold}$, and as such, must save off all internal states, and functional context that would be needed to resume correctly from the $D3_{cold}$ unpowered state.

7.2 Power Management "D State" Mappings for Modem Codecs

The ACPI and PCI Bus Power Management Interface specifications define an accepted set of device power management states (D0 – D3). A modem device driver written to comprehend these power management specifications must map each supported system-side D state to a modem Codec-specific power savings mode using the PR bits.

A high-level set of expectations for the mapping of D States to modem feature availability, power consumption,

resume latency, etc., is available in the Microsoft Communications Device Class Power Management Reference Specification** located at:

http://www.microsoft.com/hwdev/download/compmspc.rtf

Table 45 details a lower-level mapping of the modem subsystem D states to the recommended MC '97 Codec power savings PR settings.

PR<A:D> + MLNK (1-line modem Codec example)						**+12 Vmain**	**+5Vaa from +12Vmain**	**+3.3 Vmain**	**+3.3 Vaux**	**Comments**
	AC-Link	**DAC1**	**ADC1**	**Vref**	**GPIO**					
Device State	MLNK	D	C	B	A					
D0	0	0	0	0	0	On	On	On	On	All on
D1	0	***1***	***1***	0	0	On	On	On	On	-DAC, -ADC
D2	0	1	1	0	0	On	On	On	On	Same as D1
$D3_{hot}$	***1*** Note 1	1	1	Note 2	Note 2	On	On	On	On	-AC-Link
$D3_{cold}$	-	-	-	Note 2	Note 2	Off	Off	Off	On	3.3Vaux power only

Table 45. Recommended Modem Codec D state to PR bit mapping

Note 1: Codec behavior, with respect to the setting of its MLNK bit, is dependent upon whether the modem Codec was configured as the Primary or Secondary Codec. Refer to Section 7.3 below.

Note 2: GPIO (PRA) bit must be 0 to enable wake-on-ring functionality. If caller ID is supported, to enable caller ID capture, the Vref (PRB) bit must also be 0.

7.3 Power Management with Wake-up Capabilities

7.3.1 Primary MC'97 Codec and MLNK

Setting the MLNK bit must result in an AC-link halt condition (BIT_CLK stays at a logic low level). At the same time the modem Codec must also drive and hold its SDATA_IN signal low. This is similar to setting the PR4 bit for a Primary AC '97 audio Codec.

Once the MLNK bit has been set by its modem driver, BIT_CLK and SDATA_IN must remain at a logic low level until one of three events happen:

1. Low to high transition of RESET# on the AC-link
2. Warm Reset sequence signaled on the AC-link
3. A power management event occurs, such as a ring detection (pertains to SDATA_IN only)

The low to high transition of AC-link RESET# indicates resumption from the $D3_{cold}$ state where AC-link power had been removed. The sampling of this transition on the RESET# signal must effectively be treated as if observing a warm reset in the sense that no internal auxiliary powered state logic is impacted (i.e., reinitialized). Unaffected logic must include, but not necessarily be limited to, wake event status and caller ID data if supported. Resumption of normal AC-link activity must begin as though the Codec had been issued a warm reset semantic.

Warm Reset is the required resume sequence when the modem Codec has been resumed from a $D3_{hot}$ state where the AC-link had been halted yet full power had been maintained. If the modem Codec observes a Warm Reset sequence (i.e., SYNC assertion in the absence of BIT_CLK) the modem Codec shall reactivate the AC-link in the manner specified in Section 3.6.2.

If the modem Codec has been enabled to wake the system, and a power management event occurs (such as the phone ringing), then the modem Codec complies with the behavior specified in Section 6.5.2.

7.3.2 Secondary MC'97 Codec and MLNK

Setting the MLNK bit when transitioning a Secondary modem Codec to the $D3_{hot}$ state requires different behavior from the modem Codec than what is required from a Primary modem Codec.

The potential for subsequent Primary audio Codec activity requires that a Secondary modem Codec must continue to be an active participant on the AC-link as long as the AC-link continues to transact I/O frames. If enabled to generate a wake event while MLNK is set while the AC-link is still transacting I/O frames, the modem Codec must pass the GPI (Ring Indication) information normally over its SDATA_IN signal within slot 12.

If the AC-link is programmed to a PR4[15] (AC-link halted with BIT_CLK held low) the Secondary Codec must be able to detect this (e.g. one way is to snoop a writes to the Primary Codec Register 26h PR4 bit) and must, upon detecting this, drive and hold its SDATA_IN signal low. If enabled to wake-on-ring, the appropriate GPI assertion shall cause the modem Codec to transition its SDATA_IN signal from low to high signaling the wake request.

If the AC-link is transitioned to a $D3_{cold}$ state (i.e., power removed) subsequent to the MLNK bit having been set , the modem must drive and hold its SDATA_IN signal low. If enabled to wake-on-ring, the appropriate GPI assertion shall cause the modem Codec to transition its SDATA_IN signal from low to high signaling the wake request. Detecting that the AC-link has transitioned to the $D3_{cold}$ state may be accomplished by sampling the AC-link RESET# signal, given that whenever the AC-link is in the $D3_{cold}$ state RESET# is required to be actively asserted.

Once the modem Codec's SDATA_IN has been driven low for one of the two aforementioned reasons, it must remain at a logic low level until one of three events happen:

1. Low-to-high transition on AC-link RESET#
2. Warm Reset sequence signaled on the AC-link
3. A power management event occurs, such as a ring detection

The low-to-high transition of AC-link RESET# indicates resumption from the $D3_{cold}$ state where AC-link power had been removed. The sampling of this transition on the RESET# signal must effectively be treated as if observing a warm reset in the sense that no internal auxiliary powered state logic is impacted (i.e., reinitialized). Unaffected logic must include, but not necessarily be limited to, wake event status and caller ID data if supported. Resumption of normal AC-link activity must begin as though the Codec had been issued a warm reset semantic.

Warm Reset is the required resume sequence when the modem Codec has been resumed from a $D3_{hot}$ state where the AC-link had been halted yet full power had been maintained. If the Secondary modem Codec observes a Warm Reset sequence (i.e., SYNC assertion in the absence of BIT_CLK) the modem Codec shall resume normal internal operation and begin communicating over the AC-link when ready.

If the modem Codec has been enabled to wake the system, and a power management event occurs (such as the phone ringing), then the modem Codec shall comply with the behavior specified in Section 6.5.2.

7.4 Warm and Cold AC-link Reset Considerations

AC-link reset operations occur when the system is initially powered up, when resuming from a lower powered sleep state, and in response to critical subsystem failures that can only be recovered from with a reset.

The following subsections focus on the behavior of the AC-link when resuming from a low power sleep state.

7.4.1 Resume Reset Behavior

The form of reset that is signaled (if necessary) when resuming the AC-link and its Codec(s) is dependent upon the

[15] Not recommended for multiple, audio + modem, Codec configurations. See Section 7.6.

state of the Codec(s), and the power management state of the system.

Table 46, Table 47, and Table 48 break down the AC-link behavior that must occur when resuming the AC-link as a function of audio Codec device state, modem Codec device state, and system state.

Audio Codec D-State	System State (ACPI: S0-S5)	Resume activity	Comments
D0	S0	N/A	Audio active; System is operating in the Working State
D1	S0 or S1	No reset; PR bits modified	Audio idle; System is either operating in the Working State or is in S1 sleep state
D2	S0, S1, or S2	No reset; PR bits modified	Audio idle; System is either operating in the Working State, or is in S1 or S2 sleep state
D3hot	S0, S1, or S2	PR bits modified, preceded by a Warm Reset if PR4 was set	Audio idle; System is either operating in the Working State, or is in S1 or S2 sleep state
D3cold	S3, S4, or S5	Cold Reset; full Codec register and context restoration	Deep sleep state; no power to audio Codec

Table 46. Resume Reset Behavior: Audio-only

Modem Codec D-State	System State (ACPI: S0-S5)	Resume activity	Comments
D0	S0	N/A	Modem active; System is operating in the Working State
D1	S0 or S1	No reset; PR bits modified	Modem idle; System is either operating in the Working State or is in S1 sleep state
D2	S0, S1, or S2	No reset; PR bits modified	Modem idle; System is either operating in the Working State, or is in S1 or S2 sleep state
D3hot	S0, S1, or S2	PR bits modified, preceded by a Warm Reset if MLNK was set	Modem idle; System is either operating in the Working State, or is in S1 or S2 sleep state
D3cold	S3, S4, or S5	Cold reset to AC-link; modem Codec must interpret this as a warm reset; modem Codec may need partial context restoration	Deep sleep state; only auxiliary power available to the modem Codec; modem may be armed to answer the phone (except when in ACPI S5)

Table 47. Resume Reset Behavior: Modem-only

Audio Codec D-State	Modem Codec D-State	System State (ACPI: S0-S5)	Resume activity	Comments
D0	D0	S0	N/A	Audio/Modem active; System is operating in the Working State
D0	D1, D2 or D3hot	S0	No reset; modem Codec PR bits modified	Audio active, Modem idle; System is operating in the Working State
D1	D0	S0	No reset; audio Codec PR bits modified	Audio idle, modem active; System is operating in the Working State
D1	D1, D2 or D3hot	S0 or S1	No reset; audio and modem PR bits modified	Both Codecs idle; System is either operating in the Working State or in the S1 sleep state
D2	D0	S0	No reset; audio Codec PR bits modified	Audio idle, modem active; System is operating in the Working State
D2	D1, D2 or D3hot	S0, S1, or S2	No reset; audio and modem Codec PR bits modified	Both Codecs idle; System is either operating in the Working State, or in the S1 or S2 sleep state
D3hot	D0	S0	No reset; audio Codec PR bits modified	Audio Codec idle, modem active; System is operating in the Working State (note audio Codec PR4 is prohibited in Codec/system state as it would preclude normal Secondary modem Codec operation)
D3hot	D1, D2 or D3hot	S0, S1, or S2	Warm Reset if audio PR4 bit is set; otherwise audio and modem PR bits modified only	Both Codecs idle; System is either operating in the Working State, or in the S1 or S2 sleep state
D3cold	D3cold	S3, S4, or S5	Cold reset to AC-link; modem Codec must interpret this as a warm reset; full audio Codec register and context restoration, modem Codec may need partial context restoration	Deep sleep state, no power to audio Codec, only auxilairy power to modem; modem may be armed to answer the phone (except when in ACPI S5)

Table 48. Resume Reset Behavior: Audio and Modem

7.4.2 Resuming Normal AC-link Operation from S3, S4 or S5 System Sleep State

In accordance with prior revisions of the AC '97 specification, when the AC-link is unpowered, as is the case when the system is in S3, S4 or S5, the AC-link RESET# output buffer is unpowered typically leaving the RESET# signal floating at or near ground. Given the low active nature of AC-link RESET#, this presents a problem for modem Codecs that must continue to operate under auxiliary power while the system sleeps. An auxiliary powered modem Codec could be faced with what would appear to be a perpetual reset condition.

This issue is identical to the problem that any PCI-based $D3_{cold}$/PME# capable function faced when the PCI bus was programmed to B3 and the PCIRST# output buffer, being unpowered, floated around ground potential. Prior to the 3.3Vaux PCI-PM Specification updates, which require PCIRST# to be actively asserted whenever the PCI bus was in the unpowered B3 state, these PCI functions can not determine whether or not a real reset had occurred or whether the bus was unpowered and floating near ground potential.

7.4.2.1 AC-link RESET# SIGNALING REQUIREMENT

AC-link RESET# must be asserted, and actively held low whenever the system is in the S3, S4 or S5 state. Given this DC '97 Controller provides that the AC-link RESET# signal remains low at these times, an auxiliary powered

modem Codec can use the low-to-high transition on RESET# as a reliable indication that power has been reestablished on the AC-link, and that an actual resume reset has occurred.

An AC '97 2.3 Controller/Codec arrangement deployed as a PCI add-in card could have its AC-link RESET# signal follow the PCIRST# signal directly since PCIRST# will always be asserted whenever the system is sleeping in S3, S4 or S5.

7.5 Power Distribution

The AC '97 Revision 1.03 architecture was intended to enable low cost, yet high performance audio Codecs by establishing a standard split of the digital and analog portions of the audio subsystem. AC '97 Revision 2.0 brought low cost, and flexible integration of a modem Codec to the AC-link as well. The AC '97 Revision 2.2 architectural enhancements and clarifications are intended to help in merging the two subsystems with the ACPI-based Instantly Available PC power management initiative.

The desired result in applying Instantly Available PC technology to the audio and modem subsystems is to maintain AC '97 's high audio quality, while not compromising an AC-link modem Codec's ability to wake the system from a very low power, deep sleep state. To meet these objectives audio designers must have the ability to derive locally, a tightly regulated Vref supply for the Codec's DACs and ADCs. At the same time the modem Codec must have auxiliary power available to them so that they may alert the system of a ringing phone even from an ACPI S3, or S4 sleep state where 95% of all PC power is shut off.

For more details on Instantly Available PC Power Management terminology and specifications, refer to the Instantly Available PC System Power Delivery Requirements and Recommendations Specification, which can be downloaded from:

http://developer.intel.com/design/power/supply98.htm

The following subsections detail Instantly Available PC power distribution requirements for what is expected to be the three predominant AC '97 2.2 configurations.

7.5.1 MC '97 (Primary) Implementations

In support of an Instantly Available PC's "Off-yet Communicating" capabilities, modem Codecs must be capable of waking the system from a sleep state wherein the main power rails have been shut off. This implies the usage of auxiliary power.

Table 49 illustrates, all AC-link signals driven from the modem Codec, as well as all modem Codec circuitry (both digital and analog) must be powered by an auxiliary 3.3 V supply (3.3 Vdual).

	+3.3 Vmain	+5 Vmain	+12 Vmain	+3.3 Vdual (3.3 Vaux)
AC-link (Codec outputs) • BIT_CLK • SDATA_IN				✓ ✓
AC-link (contrl. outputs) • SYNC • SDATA_OUT • RESET#	✓ ✓			✓
MC'97 digital logic				✓
MC'97 analog circuitry				✓ (note 1)
Note 1: Modem codecs that do not support hardware capture of caller ID during ACPI S3 or S4 states may alternatively power their analog circuitry with either 3.3 Vmain or 5 Vmain.				

Table 49. Power Distribution: MC '97 as the Primary (Modem-Only configuration)

7.5.2 AC '97 (Primary) + MC '97 (Secondary) Implementations

Table 50 depicts the power distribution that enables both high quality audio and "Off-yet Communicating" modem operation.

	+3.3 Vmain	+5V main	+5 Vaa from +12 Vmain	+3.3 Vdual (3.3 Vaux)
AC-link (Codec outputs) • BIT_CLK • SDATA_IN(audio) • SDATA_IN(modem)	✓ ✓			✓
AC-link (contr. outputs) • SYNC • SDATA_OUT • RESET#	✓ ✓			✓
Audio digital logic	✓			
Audio analog circuitry		✓ (mobile option)	✓	
Modem digital logic				✓
Modem analog circuitry				✓ (note1)
Modem wake logic				✓
Note 1: Modem codecs that do not support hardware capture of caller ID during ACPI S3 or S4 states may alternatively power their analog circuitry with either 3.3 Vmain or 5 Vmain. All audio Codec driven AC-link signals, as well as all other digital logic associated with the audio subsystem, must be powered by 3.3 Vmain. It is recommended that the audio subsystem locally regulate +12 Vmain down to +5 Vaa for use by its analog circuitry.				

Table 50. Power Distribution: Split Codec Partitioned Audio-plus-Modem

All modem Codec driven AC-link signals, as well as all other digital logic and analog caller ID capture circuitry must be powered by +3.3 Vdual, enabling an Instantly Available PC.

This power distribution scheme enables the audio Codec to be powered from typical working state voltage sources

that are shut off when the PC enters an ACPI sleep state of S3, S4 or S5. Additionally it enables the modem Codec to power its wake logic when in an S3, S4 or S5 ACPI sleep state.

7.5.3 AMC ‘97 (Primary) Implementations

The AMC ‘97 combination Codec must implement the same power distribution strategy as for the split partitioned AC + MC Codec configuration. This imposes a requirement on AMC ‘97 Codec designs, in that they are designed with split power wells enabling multi-voltage power distribution for different sections of the component. Please refer to Table 50.

7.6 AC + MC clocking considerations

In an AC ‘97 compliant multiple audio + modem Codec configuration[16] the AC ‘97 Digital Controller and Secondary modem Codec depend upon the Primary audio Codec delivering BIT_CLK to them for proper modem operation.

Therefore when the modem is in the active state (i.e., D0) the audio driver must never shut off the BIT_CLK by setting the audio Codec PR4 bit. In addition, the audio and modem drivers must be mutually exclusive of each other, meaning that the audio driver is limited to managing the audio Codec hardware only and must not interact directly with the modem driver or modem Codec hardware. To avoid this BIT_CLK clocking issue it is recommended that the audio Codec PR4 bit NOT be set in multiple audio + modem Codec configurations.

AC ‘97 Multiple Codec Clocking Recommendations:

1. An audio driver should never set the PR4 bit in a multiple audio + modem Codec configuration. This ensures that the BIT_CLK never stops when the PC is in the working state.
2. Primary Codecs should implement the following clocking options:
    a. Using an external 24.576MHz crystal between the XTAL_IN and XTAL_OUT pins.
    b. An external oscillator signal present on XTAL_IN with support for 14.318MHz or 24.576 MHz frequencies.
    c. An external oscillator input of frequency 12.288MHz on BIT_CLK.

    All of the above cases (a-c) must result in BIT_CLK running at 12.288MHz.
3. Secondary Codecs use BIT_CLK (and SYNC) input for all AC-link transaction timings
4. Secondary modem Codecs should support an additional, auxiliary powered clock input (XTAL or OSC) that is used for hardware caller ID functionality while the system is in an ACPI S3, S4 or S5 sleep state (i.e., for use at times when the AC-link, including BIT_CLK, is powered off)

Audio-only multiple Codec implementations should have no BIT_CLK clocking issues as all of the AC-link Codecs are managed by the same device driver.

7.7 Resume Latency: Device Driver Considerations

Device drivers should be written to distinguish between a cold boot, and a resume event from S3, S4 or S5. By making this distinction a driver could be written to minimize its contribution to the system’s resume latency.

Device drivers should not use the same boot time initialization code sequence when resuming from S3, S4, or S5 sleep states.

[16] An AC ’97 audio Codec with a physically separate MC ’97 modem Codec or, a combined AMC ’97 audio/modem Codec.

8. Testability

8.1 Activating the Test Modes

SYNC	SDATA_OUT	Description
0	0	Normal AC ’97 operation
0	1	ATE Test Mode
1	0	Vendor Test Mode
1	1	Reserved

Table 51. Test Mode Activation

AC ‘97 has two test modes. One is for ATE in circuit test and the other is for vendor-specific tests. All AC-link signals are normally low through the trailing edge of RESET#. When coming out of RESET, an AC ‘97 Codec enters the ATE in circuit test mode if SDATA_OUT is sampled high at the trailing edge of RESET#, and enters the vendor-specific test mode if SYNC is sampled high at the trailing edge of RESET#.

These cases will not occur during typical operating conditions.

Regardless of the test mode, the AC ‘97 Controller must issue a cold reset to resume normal operation of the AC ‘97 Codec.

8.2 Test Mode Functions

8.2.1 ATE in circuit test mode

When AC ‘97 is placed in the ATE test mode, its digital AC-link outputs and digital I/O are driven to a high impedance state (internal pull-ups for digital I/O pins must be disabled in this mode). This allows ATE in circuit testing of the AC ‘97 Controller.

Recommended pins:

- BIT_CLK
- SDATA_IN
- EAPD
- SPDIF_OUT
- ID0, ID1
- GPIOs

8.2.2 Vendor-specific test mode

This is left up to the individual vendors.

9. Digital DC and AC Characteristics

9.1 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Power Supply	DVdd	3.135	3.3	3.465	V
Input voltage range	V_{in}	-0.30	-	DVdd + 0.30	V
Low level input voltage	V_{il}	-	-	0.35 x DVdd	V
High level input voltage	V_{ih}	0.65 x DVdd	-	-	V
High level output voltage	V_{oh}	0.90 x DVdd	-	-	V
Low level output voltage	V_{ol}	-	-	0.10 x DVdd	V
Input Leakage Current (AC-link inputs)	-	-10	-	10	µA
Output Leakage Current (Hi-Z'd AC-link outputs)	-	-10	-	10	µA
Input/Output Pin Capacitance	-			7.5	pF

Table 52. 3.3 V DC Characteristics

AC '97 recommends new Controller and Codec designs support 3.3 V digital operation as specified in Table 52.

9.2 AC Timing Characteristics

9.2.1 Reset Timing

The AC '97 Architecture defines three types of reset that an AC '97 compatible Codec must comprehend:

1. Cold reset — RESET# — Complete hardware reset; all registers default state
2. Register reset - Audio — write to 00h — All audio registers default state
   Register reset - Modem — write to 3Ch — Al modem registers default state
3. Warm reset — SYNC w/o BITCLK — Re-activates AC-link; no change to register values

Registers should take their default values after Cold or Register reset, but not Warm reset.

9.2.1.1 Recommended AC-link Cold Reset Behavior and Timing

As the popularity of OEM riser card audio increases (see the Communication and Networking Riser Specification), so does the potential for motherboard audio and riser card audio electrical conflicts[17]. To minimize the potential for damage from such conflicts, it is recommended that audio Codecs place their BIT_CLK and SDATA_IN pins in a tri-state mode (instead of driving them low) while RESET# is active low. Figure 29 provides the recommended timing:

[17] However, for reliability, compatibility, and ease of use concerns, Intel does NOT recommend any configuration of OEM riser card audio that disables motherboard audio and jacks.

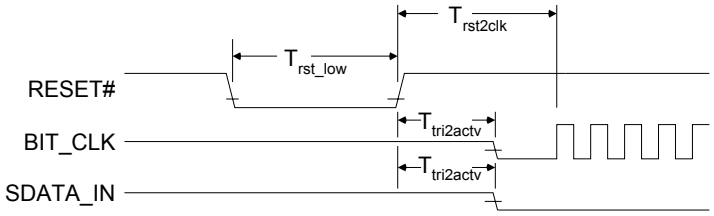


Figure 29. Cold Reset timing diagram when the codec is supplying the BIT_CLK signal

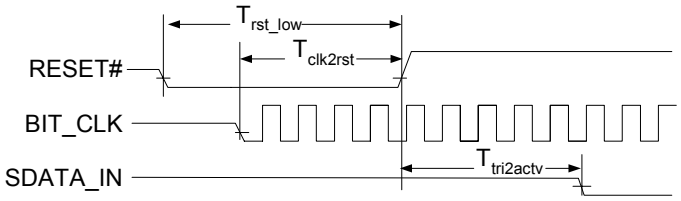


Figure 30 Cold Reset timing diagram when BIT_CLK is being provided by an external source.

Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	Trst_low	1.0	-	-	µs
RESET# inactive to SDATA_IN or BIT_CLK active delay	Ttri2actv	-	-	25	ns
RESET# inactive to BIT_CLK startup delay	Trst2clk	162.8	-	400[18]	ns
BITCLK active to RESET# asserted	Tclk2rst	0.416	-	-	µs

Table 53. Cold Reset timing parameters

9.2.1.2 Warm Reset Timing

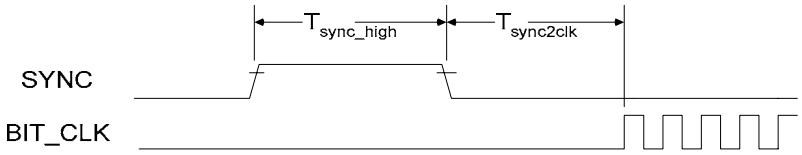


Figure 31. Warm Reset timing diagram

[18] Note that this requirement, in combination with the BITCLK startup to Codec Ready Assertion maximum of 400us (defined in section 4.4.1), implies that the first assertion of Codec Ready could be delayed up to 800us after RESET# deassertion.

Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	µs
SYNC inactive to BIT_CLK startup delay	$T_{sync2clk}$	162.8	-	-	ns

Table 54. Warm Reset timing parameters

Please note that this minimum SYNC pulse width pertains to warm reset only, during normal operation SYNC is asserted for the entire tag phase (16 BIT_CLK times).

9.2.2 AC-link Clocks

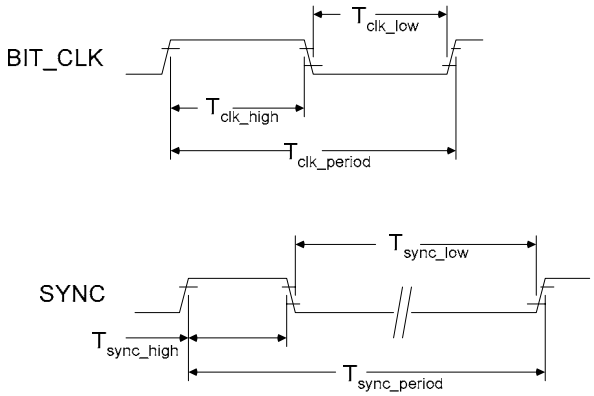


Figure 32. BIT_CLK and SYNC Timing diagram

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (note 2)	Tclk_high	36	40.7	45	ns
BIT_CLK low pulse width (note 2)	Tclk_low	36	40.7	45	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	Tsync_period	-	20.8	-	µs
SYNC high pulse width	Tsync_high	-	1.3	-	µs
SYNC low pulse width	Tsync_low	-	19.5	-	µs
Note 1: 47.5-75 pF external load as per Table 62 Note 2: Worst case duty cycle restricted to 45/55					

Table 55. BIT_CLK and SYNC Timing Parameters

9.2.3 Data Output and Input Times

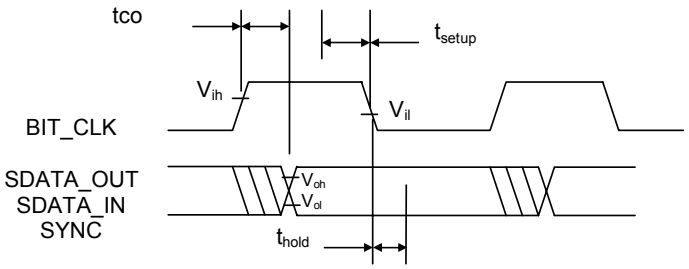


Figure 33. Data Output and Input Timing Diagram

Parameter	Symbol	Min	Typ	Max	Units
Output Valid Delay from rising edge of BIT_CLK	tco	-	-	15	ns
Note: 47.5-75pF external load as per Table 62					

Table 56. AC-link Output Valid Delay Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Input Setup to falling edge of BIT_CLK	t_{setup}	10	-	-	ns
Input Hold from falling edge of BIT_CLK	t_{hold}	10	-	-	ns

Table 57. AC-link Input Setup and Hold Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK combined rise or fall plus flight time (Primary Codec to Controller or Secondary)		-	-	7	ns
SDATA combined rise or fall plus flight time (Output to Input)		-	-	7	ns
Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purposes					

Table 58. AC-link Combined Rise or Fall plus Flight Timing Parameters

The original AC '97 1.03 Specification specified SDATA and SYNC to BIT_CLK setup and hold times for point-to-point Controller to Codec connections. The multiple Codec configurations defined by AC '97 2.x introduce Secondary Codecs that derive their AC-link timing from a Primary Codec's BIT_CLK. Riser solutions under development define system implementations where AC-link signal trace lengths can run up to ~15 inches, with total external capacitive loads of 50 pF or greater. Both of these can impact SDATA and SYNC to BIT_CLK timing relationships, as well as the strength of the AC-link output pin drivers.

The typical Controller or Codec updates an AC-link output signal on the rising edge of BIT_CLK, drives it valid prior to BIT_CLK falling, and holds it valid for the entire duration of BIT_CLK low. The typical Controller or Codec latches AC-link input signals on the falling edge of BIT_CLK. The new Output Valid Delay timing parameters and reduced Input Setup and Hold times help to allow AC-link operation for multiple Codec and/or riser implementations.

Rise and Fall times, flight times, Output Valid Delay, Input Setup and Hold, and worst case capacitive loads (see Section 9.2.7) should be used together for modeling of the AC-link output pin drivers.

For example, the following worst case scenario situates the Primary Codec along with a Secondary Codec on a riser 15 inches from the Controller. The AC-link BIT_CLK, SYNC, and SDATA_OUT signals are loaded with ~55 pF external capacitance. The Primary drives BIT_CLK to the Controller with a 7 ns combined rise plus flight time, the Controller delays 15 ns in driving SDATA_OUT valid (includes the 7 ns return combined rise or fall plus flight time), and the Codec requires stable data 10 ns prior to latching. Assuming the minimum BIT_CLK high time of 36 ns (provided by the new 45/55 duty cycle requirement) yields:

$$36 - (7 + 15 + 10) = 4 \text{ ns margin}$$

9.2.4 Signal Rise and Fall Times

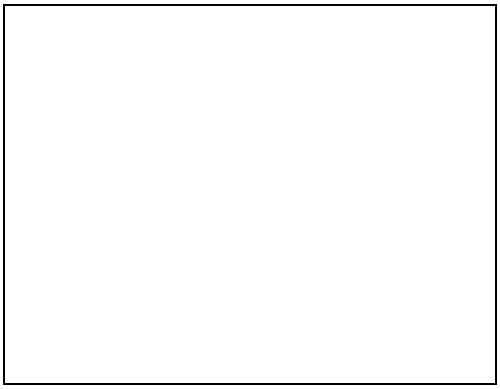


Figure 34. Signal Rise and Fall Timing Diagram

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time (Note 1)	$Trise_{clk}$	-	-	6	ns
BIT_CLK fall time (Note 1)	$Tfall_{clk}$	-	-	6	ns
SYNC rise time (Note 2)	$Trise_{sync}$	-	-	6	ns
SYNC fall time (Note 2)	$Tfall_{sync}$	-	-	6	ns
SDATA_IN rise time (Note 3)	$Trise_{din}$	-	-	6	ns
SDATA_IN fall time (Note 3)	$Tfall_{din}$	-	-	6	ns
SDATA_OUT rise time (Note 2)	$Trise_{dout}$	-	-	6	ns
SDATA_OUT fall time (Note 2)	$Tfall_{dout}$	-	-	6	ns

Note 1: BIT_CLK rise/fall times with an external load of 75 pF

Note 2: SYNC and SDATA_OUT rise/fall times with a external load of 75 pF

Note 3: SDATA_IN rise/fall times with an external load of 60 pF

Note 4: Rise is from 10% to 90% of Vdd (V_{ol} to V_{oh})

Note 5: Fall is from 90% to 10% of Vdd (V_{oh} to V_{ol})

Table 59. Signal Rise and Fall Time Parameters

AC '97 2.3 maintains the original specified BIT_CLK, SYNC, SDATA_OUT, and SDATA_IN signal rise and fall times. These signals must also meet the Output Valid Delay time with respect to the rising edge of BIT_CLK specified in Table 56.

Modeling of the AC-link output pin drivers should include rise and fall times, flight times, and external capacitive and inductive loads, which could be as large as 75 pF. Special consideration should be given to the BIT_CLK output pin driver for any Primary Codec that is designed to operate in multiple Codec and/or riser implementations. In addition, the same consideration should be given to SYNC and SDATA_OUT output pin drivers for any AC '97 Controller that is designed to operate in multiple Codec and/or riser implementations.

System designers should be aware that with the increased driver strengths required to meet the above rise/fall times (with specified load), point-to-point routings with low total capacitive loads might require EMI reduction techniques, such as series resistors.

9.2.5 AC-link Low Power Mode Timing

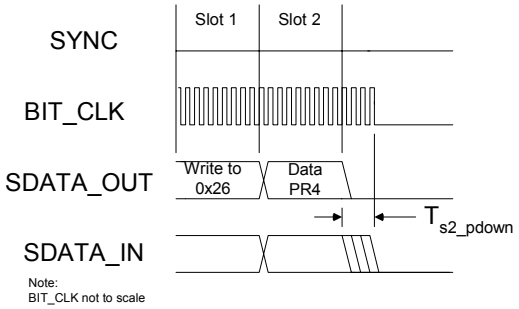


Figure 35. AC-link low power mode timing diagram

Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdown	-	-	1.0	µs

Table 60. AC-link low power mode timing parameters

9.2.6 ATE Test Mode

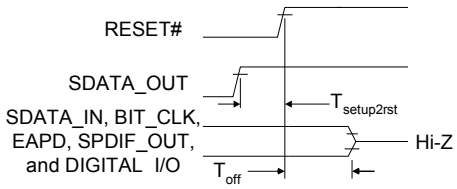


Figure 36. ATE test mode timing diagram

Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	Tsetup2rst	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	Toff	-	-	25.0	ns

Table 61. ATE test mode timing parameters

All AC-link signals are normally low through the trailing edge of RESET#.

1. Bringing SDATA_OUT high for the trailing edge of RESET# causes an AC '97 Codec's AC-link outputs and Digital I/O to go high impedance which is suitable for ATE in circuit testing.
2. Bringing SYNC high for the trailing edge of RESET# causes an AC '97 Codec to enter a vendor-specific internal test mode. This mode has no effect on AC '97 AC-link output signal levels.
3. Bringing both SDATA_OUT and SYNC high for the trailing edge of RESET# is reserved.

Once either of the two test modes has been entered, AC '97 must be issued another RESET# with all AC-link signals low to return to the normal operating mode. For additional details on AC '97 test modes, refer to Section 8.1.

9.2.7 AC-link IO Pin Capacitance and Loading

The utilization and popularity of multiple Codec configurations and OEM riser card audio is growing, and AC '97 2.3 Controllers and Codecs intended for such uses need to be designed accordingly.

In multiple Codec and riser implementations, the AC '97 Controller drives SYNC and SDATA_OUT to two or more destinations. The Controller's SYNC and SDATA_OUT output pin drivers need to meet AC-link timing requirements when loaded by the total capacitance on each of these outputs.

In multiple Codec implementations, the Primary AC '97 Codec drives BIT_CLK to two or more destinations. The Codec's BIT_CLK output pin driver needs to meet AC-link timing requirements when loaded by the total capacitance on this output.

The following factors contribute to total capacitance:

- Controller or Codec output pin capacitance (7.5 pF max per AC '97 2.3)
- Codec or Controller input pin capacitance (7.5 pF max per AC '97 2.3)
- Total trace length capacitance on motherboard plus riser[19] (estimated 2.5 pF per inch)
- IO connectors, such as motherboard to riser (estimated 2.5 pF)

AC '97 2.3 compliance requires that the following Controller and Codec *input and output pins* have a maximum of 7.5 pF capacitance. This applies to:

- Controller BIT_CLK and SDATA_IN[0-3] inputs
- Primary and Secondary Codec, as well as Controller SYNC and SDATA_OUT inputs
- Secondary Codec BIT_CLK input

AC '97 2.3 compliance strongly recommends the following Controller and Codec AC-link output pin drivers be of sufficient strength to meet AC-link timing requirements for the following specified external[20] capacitive loads in 1-4 Codec implementations, as per the following three tables:

[19] Motherboard plus riser trace lengths, especially in multiple Codec implementations such as AC down (motherboard) and MC up (riser), could exceed ~15 inches, particularly in NLX form factor designs.
[20] In addition to these external capacitive loads, additional allowance must be made for the particular Controller or Codec (internal device characteristic).

RESET, SYNC, & SDATA_OUT	1 Codec	2 Codecs	3 Codecs	4 Codecs
Controller Output Pin Capacitance	7.5pF	7.5pF	7.5pF	7.5pF
Motherboard Trace Capacitance (Note 1)	30pF	30pF	30pF	30pF
Codec Input Pin Capacitance (Note 2)	7.5pF	15pF	22.5pF	30pF
Riser Connector Capacitance	2.5pF	2.5pF	2.5pF	2.5pF
CNR Trace Capacitance (Notes 3 & 4)	0pF	7.5pF	12.5pF	15pF
Total Capacitance driven by output pin	47.5pF	62.5pF	75pF	85pF
Note 1 – Motherboard Trace Capacitance assumed to be 12 inches of trace length at ~2.5pF per inch Note 2 – Codec Input Pin Capacitance based off of 7.5pF per input pin, as specified in AC '97 2.3 Note 3 – CNR Trace Capacitance assumed to be 2.5pF per inch with 3 inches for 2nd Codec, 5 inches for 3rd Codec, and 6 inches for 4th Codec Note 4 – 1st Codec is assumed to be on the motherboard				

Table 62. AC-link Controller output pin driver loading

BIT_CLK	1 Codec	2 Codecs	3 Codecs	4 Codecs
Codec Output Pin Capacitance	7.5pF	7.5pF	7.5pF	7.5pF
Motherboard Trace Capacitance (Note 1)	30pF	30pF	30pF	30pF
Codec Input Pin Capacitance (Note 2 & 4)	0pF	7.5pF	15pF	22.5pF
Controller Input Pin Capacitance	7.5pF	7.5pF	7.5pF	7.5pF
Riser Connector Capacitance	2.5pF	2.5pF	2.5pF	2.5pF
CNR Trace Capacitance (Notes 3 & 4)	0pF	7.5pF	12.5pF	15pF
Total Capacitance driven by output pin	47.5pF	62.5pF	75pF	85pF
Note 1 – Motherboard Trace Capacitance assumed to be 12 inches of trace length at ~2.5pF per inch Note 2 – Codec Input Pin Capacitance based off of 7.5pF per input pin, as specified in AC '97 2.3 Note 3 – CNR Trace Capacitance assumed to be 2.5pF per inch with 3 inches for 2nd Codec, 5 inches for 3rd Codec, and 6 inches for 4th Codec Note 4 – 1st Codec is assumed to be on the motherboard and is the Codec driving the BIT_CLK signal				

Table 63. AC-link Codec BIT_CLK Output pin driver loading

SDATA_IN	1 Codec	2 Codecs	3 Codecs	4 Codecs
Codec Output Pin Capacitance	7.5pF	7.5pF	7.5pF	7.5pF
Motherboard Trace Capacitance (Note 1)	30pF	30pF	30pF	30pF
Controller Input Pin Capacitance	7.5pF	7.5pF	7.5pF	7.5pF
Riser Connector Capacitance	2.5pF	2.5pF	2.5pF	2.5pF
CNR Trace Capacitance (Notes 2 & 3)	0pF	7.5pF	12.5pF	15pF
Total Capacitance driven by output pin	47.5pF	55pF	60pF	62.5pF
Note 1 – Motherboard Trace Capacitance assumed to be 12 inches of trace length at ~2.5pF per inch Note 2 – CNR Trace Capacitance assumed to be 2.5pF per inch with 3 inches for 2nd Codec, 5 inches for 3rd Codec, and 6 inches for 4th Codec Note 3 – 1st Codec is assumed to be on the motherboard and is the Codec driving the BIT_CLK signal				

Table 64. AC-link Codec SDATA_IN Output pin driver loading

10. Analog Performance Characteristics

(Test conditions unless otherwise noted: $T_{ambient}$ = 25^{0}C; DVdd = 3.3 V +/- 5%; AVdd = 5.0 V +/- 5%; 1 kHz input

sine wave; Sample Frequency = 48 kHz; 0 dB = 1Vrms, 10KΩ/50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB attenuation; tone and 3D disabled)

Parameter	Min	Typ	Max	Units
Full Scale Input Voltage:				
Line Inputs	-	1.0	-	Vrms
Mic Inputs[1]	-	0.1	-	
Full Scale Output Voltage:	-	-	-	
Line Output	-	1.0	-	Vrms
Headphone Output	-	-	1.41	
Analog S/N:				
CD to LINE_OUT	90	-	-	dB
Other to LINE_OUT	-	85	-	
Analog Frequency Response[2]	20	-	20,000	Hz
Digital S/N[3]				
D/A	85	90	-	dB
A/D	75	80	-	
Total Harmonic Distortion:				
Line Output[4]	-	-	0.02	%
Headphone Output[5]	-	-	1.0	
D/A & A/D Frequency Response[6]	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	□	Hz
Stop Band Rejection[7]	-74	-	-	dB
Out-of-Band Rejection[8]	-	-40	-	dB
Group Delay	-	-	1	ms
Power Supply Rejection Ratio (1 kHz)	-	-40	-	dB
Crosstalk between Inputs channels	-	-	-70	dB
Spurious Tone Reduction	-	-100	-	dB
Attenuation, Gain Step Size[9]	-	1.5	-	dB
Input Impedance	10	-	-	kΩ
Input Capacitance	-	7.5	-	pF
Vrefout	-	2.25-2.75	-	V

Table 65. AC '97 analog performance characteristics

Notes:
(1) With +20 dB Boost on, 1.0 Vrms with Boost off
(2) ±1dB limits
(3) The ratio of the rms output level with 1 kHz full scale input to the rms output level with all zeros into the digital input.
Measured "A wtd" over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
(4) 0 dB gain, 20 kHz BW, 48 kHz Sample Frequency

(5) +3 dB output into 32 Ω load
(6) ±0.25 dB limits
(7) Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
(8) The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth of 28.8 to 100 kHz, with respect to a 1VRMS DAC output.
(9) Gain step size 1.5 dB is true for all attenuators except for PC_BEEP, which has 3.0 dB step size.

Appendix A. AC ‘97 Register Set Summary

The AC ‘97 Register space supports 64 16-bit registers using even 7-bit addresses.

- Registers 00h – 26h are dedicated to the baseline audio feature set
- Registers 28h – 3Ah are dedicated to the extended audio feature set
- Registers 3Ch – 58h are dedicated to the standardized modem feature set
- Registers 5Ah – 7Ah are reserved for vendor-specific functionality
- Registers 7Ch and 7Eh are dedicated to Microsoft Plug and Play Vendor ID** (3 bytes) and vendor specific device ID (8-bits)

All reserved bits (marked x) should be read as zero, and zeros should be written to these bits by Controllers and software. All AC ‘97 Codecs should respond with 0 to accesses of odd-numbered registers instead of aliasing them to the next lower even-numbered register. As a result, odd-numbered registers can be reserved for future expansion.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	na
02h	Master Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
04h	Aux Out Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
06h	Mono Volume	Mute	X	X	X	X	X	X	X	X	X	MM5	MM4	MM3	MM2	MM1	MM0	8000h
08h	Master Tone	X	X	X	X	BA3	BA2	BA1	BA0	X	X	X	X	TR3	TR2	TR1	TR0	0F0Fh
0Ah	PC Beep Volume	Mute	X	X	X	F7	F6	F5	F4	F3	F2	F1	PV3	PV2	PV1	PV0	X	x000h
0Ch	Phone Volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20 dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
1Eh	Record Gain Mic	Mute	X	X	X	X	X	X	X	X	X	X	X	GM3	GM2	GM1	GM0	8000h
20h	General Purpose	POP	ST	3D	LD	DRSS1	DRSS0	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
22h	3D Control	X	X	X	X	CR3	CR2	CR1	CR0	X	X	X	X	DP3	DP2	DP1	DP0	0000h
24h	RESERVED	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
26h	Powerdown Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	na
28h-3Ah	Extended Audio	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
3Ch-58h	Extended Modem	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	B
5Ah-7Ah	Vendor Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	na
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	na

Table 66. AC '97 Baseline Audio Register Map

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	ID1	ID0	x	x	REV1	REV0	AMAP	LDAC	SDAC	CDAC	DSA1	DSA0	VRM	SPDIF	DRA	VRA	xxxxh
2Ah	Ext'd Audio Stat/Ctrl	VCFG	PRL	PRK	PRJ	PRI	**SPCV**	MADC	LDAC	SDAC	CDAC	**SPSA1**	**SPSA0**	VRM	**SPDIF**	DRA	VRA	xxxxh
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
2Eh	PCM Surr DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
30h	PCM LFE DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM L/R ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
34h	MIC ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
36h	Center/LFE Volume	Mute	x	*LFE5*	LFE4	LFE3	LFE2	LFE1	LFE0	Mute	x	*CNT5*	CNT4	CNT3	CNT2	CNT1	CNT0	8080h
38h	Surr Volume	Mute	x	*LSR5*	LSR4	LSR3	LSR2	LSR1	LSR0	Mute	x	*RSR5*	RSR4	RSR3	RSR2	RSR1	RSR0	8080h
3Ah	S/PDIF Control	V	DRS	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/AUDIO	PRO	2000h

Table 67. AC '97 Extended Audio Register Map

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Ch	Extended Modem ID	ID1	ID0	x	x	x	x	x	x	x	x	X	CID2	CID1	HSET	LIN2	LIN1	xxxxh
3Eh	Ext'd Modem Stat/Ctrl	PRH	PRG	PRF	PRE	PRD	PRC	PRB	PRA	HDAC	HADC	DAC2	ADC2	DAC1	ADC1	MREF	GPIO	xxxxh
40h	Line 1 DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
42h	Line 2 DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
44h	Handset DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
46h	Line 1 DAC/ADC Level	Mute	x	x	x	DAC3	DAC2	DAC1	DAC0	Mute	x	X	x	ADC3	ADC2	ADC1	ADC0	8080h
48h	Line 2 DAC/ADC Level	Mute	x	x	x	DAC3	DAC2	DAC1	DAC0	Mute	x	X	x	ADC3	ADC2	ADC1	ADC0	8080h
4Ah	Handset DAC/ADC Level	Mute	x	x	x	DAC3	DAC2	DAC1	DAC0	Mute	x	X	x	ADC3	ADC2	ADC1	ADC0	8080h
4Ch	GPIO Pin Config	GC15	GC14	GC13	GC12	GC11	GC10	GC9	GC8	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	xxxxh
4Eh	GPIO Pin Polarity/Type	GP15	GP14	GP13	GP12	GP11	GP10	GP9	GP8	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	FFFFh
50h	GPIO Pin Sticky	GS15	GS14	GS13	GS12	GS11	GS10	GS9	GS8	GS7	GS6	GS5	GS4	GS3	GS2	GS1	GS0	0000h
52h	GPIO Pin Wake-up	GW15	GW14	GW13	GW12	GW11	GW10	GW9	GW8	GW7	GW6	GW5	GW4	GW3	GW2	GW1	GW0	0000h
54h	GPIO Pin Status	GI15	GI14	GI13	GI12	GI11	GI10	GI9	GI8	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0	xxxxh
56h	Misc Mdm AFE Stat/Ctrl	CID2	CID1	CIDR	MLNK	x	HSB2	HSB1	HSB0	x	L2B2	L2B1	L2B0	x	L1B2	L1B1	L1B0	x000h
58h	RESERVED	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Table 68. AC '97 Extended Modem Register Map